WORKSHOP SCIENTIFIC PROGRAM (Tentative)

September 25 (Thursday), 2008

4th International WorkShop on New Group IV Semiconductor Nanoelectronics

Sep. 25(Thu.) - 27(Sat.), 2008

Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., Sendai, Japan

Tutorial Lecture 14:00-15:45 (4F Conference Room)

14:00-15:45 **"0.13 µm SiGe BiCMOS Technology for Radio-Frequency Applications"**, Bernd Tillack[1,2], Holger Rücker[1], Bernd Heinemann[1], Alexander Fox[1], Dieter Knoll[1] and Wolfgang Mehr[1], [1]IHP, Germany, [2]Technische Universität Berlin, Germany · · · 1

WORKSHOP SCIENTIFIC PROGRAM (Tentative)
September 26 (Friday), 2008

Session 0: Opening 12:50-13:00 (4F Conference Room)

12:50-13:00 **Introductory**
Junichi Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

Session I: Invited Presentation (1) 13:00-14:30 (4F Conference Room)

13:00-13:30 I-01:
"Si passivation in Ge pMOSFETS: further developments and understanding", ・・・ 3
Matty Caymax, Jerome Mitard, Koen Martens, Lijun Yang, Geoffrey Pourtois, Wilfried Vandervorst and Marc Meuris
IMEC, Belgium

13:30-14:00 I-02:
"Epitaxial growth of ferromagnetic Mn_5Ge_3 on Ge(111) and (001) substrates", ・・・ 5
V. Le Thanh, S. Olive-Mendez, A. Spiesser, L.A. Michez, A. Glachant and J. Derrien,
Centre Interdisciplinaire de Nanoscience de Marseille (CINaM- CNRS 3118), Aix-Marseille Université, France

14:00-14:30 I-03:
"Patterned SiGe heterostructures through UV Excimer Laser radiation", ・・・ 7
S. Chiussi[1], F. Gontad[1], E. Rebollar[1], J.C. Conde[1], C. Serra[1,2], J. Serra[1], P. González[1] and B. León[1],
[1]Departamento de Física Aplicada, E.T.S.I.Industriales, Universidade de Vigo, Spain,
[2]C.A.C.T.I., Universidade de Vigo, Spain

Session II: Regular Presentation (1) 14:30-15:10 (4F Conference Room)

14:30-14:50 O-01:
"Visible photocurrent measurements in Ge quantum dots", ・・・ 9
P. Castrucci[1], C. Scilletta[1], E. Speiser[1], M. Scarselli[1] and M. De Crescenzi[1], A. Ronda[2] and I. Berbezier[2],
[1]Dipartimento di Fisica, Unita' CNISM, Universita' di Roma Tor Vergata, France,
[2]L2MP UMR CNRS 6137, Faculté des Sciences et Techniques, Campus de Saint Jerome, France

14:50-15:10 O-02:
"Low-Temperature-Processing Metal-Oxide-Semiconductor (MOS) Structure Solar Cell Prepared by Cost-Effective Anodization Technique", ・・・ 11
Chih-Yao Wang and Jenn-Gwo Hwu,
Graduate Institute of Electronics Engineering /Department of Electrical Engineering, National Taiwan University, Taiwan, R.O.C.

15:10-15:30 **Break**

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Session III: Regular Presentation (2)　15:30-17:10 (4F Conference Room)

15:30-15:50 O-03:
"Influence of HCl on the Low Temperature SiGe Selective Epitaxial Growth using SiH_4-GeH_4-B_2H_6-H_2-HCl Gas Mixture by LP-CVD System", ・・・ 13
Y. Shimamune[1], M. Fukuda[2], M. Nishikawa[2], H. Maekawa[1], N. Tamura[1], T. Mori[2], M. Kase[2] and S. Fukuyama[1],
[1]Fujitsu Laboratories Ltd., Japan,
[2]Fujitsu Microelectronics Ltd., Japan

15:50-16:10 O-04:
"Quantitative strain estimation using C-V characteristics of strained Si MOS capacitor", ・・・ 15
Mitsuhiro Inagaki and Satoru Matsumoto,
Faculty of Science and Technology, Keio University, Japan

16:10-16:30 O-05:
"Mechanism of strain relaxation in SiGe films grown on Si(110) substrates", ・・・ 17
Keisuke Arimoto[1], Masato Watanabe[1], Toshihiko Yajima[1], Junji Yamanaka[1], Kiyokazu Nakagawa[1], Kentarou Sawano[2], Yasuhiro Shiraki[2], Noritaka Usami[3] and Kazuo Nakajima[3],
[1]Center for Crystal Science and Technology, University of Yamanashi, Japan,
[2]Musashi Institute of Technology, Japan,
[3]Institute for Materials Research, Tohoku University, Japan

16:30-16:50 O-06:
"Analysis of Uniaxial Tensile Strain in Microfabricated Ge/$Si_{1-x}Ge_x$ Structures on Si(001) Substrates", ・・・ 19
Takuya Mizutani[1], Osamu Nakatsuka[1], Akira Sakai[2], Hiroki Kondo[1] and Sigeaki Zaima[1],
[1]Graduate School of Eng., Nagoya University, Japan,
[2]Graduate School of Eng. Sci., Osaka University, Japan

16:50-17:10 O-07:
"Low temperature pre-epi treatment: critical parameters to control interface contamination", ・・・ 21
Roger Loo[1], Andriy Hikavyy[1], Frederik Leys[1], Masayuki Wada[2], Brecht De Vos[1], Antoine Pacco[1], Mireia Bargallo Gonzalez[1], Eddy Simoen[1], Peter Verheyen[1], Wendy Vanherle[1] and Matty Caymax[1],
[1]IMEC, Belgium, [2]Dainippon Screen Mfg. Co., Ltd., Japan

Banquet　19:00-20:30 (Hotel Bel Air 1F)

WORKSHOP SCIENTIFIC PROGRAM (Tentative)
September 27 (Saturday), 2008

Session IV: Short Oral Presentation 10:00-11:00 (4F Conference Room)

10:00-10:04 P-01:
"Strain Engineering by Si:C / Si / SiGe Deposition into Cavity Formed by Sacrificial SiGe Layer Etching using HCl", ・・・ 23
Yuji Yamamoto, Klaus Köpke, Günter Weidner and Bernd Tillack,
IHP, Germany

10:04-10:08 P-02:
"Transition from Epitaxial to Polycrystalline Selective Si Deposition Induced by B-Atomic Layer Doping", ・・・ 25
Yuji Yamamoto[1], Klaus Köpke[1], Oksana Fursenko[1], Günter Weidner[1],
Junichi Murota[2] and Bernd Tillack[1],
[1]IHP, Germany, [2]Res. Inst. Electr. Comm., Tohoku University, Japan

10:08-10:12 P-03:
"Formation and Characterization of Compositionally Step-graded $Ge_{1-x}Sn_x$ Buffer Layers for Tensile-strained Ge Layers", ・・・ 27
Yosuke Shimura[1], Norimasa Tsutsui[1], Osamu Nakatsuka[1], Akira Sakai[2] and
Shigeaki Zaima[1],
[1]Graduate School of Eng., Nagoya University, Japan,
[2]Graduate School of Eng. Sci., Osaka University, Japan

10:12-10:16 P-04:
"Reduction in Surface Roughness of Epitaxial Ge on Si by Hydrogen Annealing", ・・・ 29
Shin-ichi Kobayashi,
Department of System Engineering and Information Technology, Tokyo Polytechnic University, Japan

10:16-10:20 P-05:
"Microstructure change of an As+ ion-implanted $Si_{0.99}C_{0.01}$/Si by rapid thermal annealing", ・・・ 31
Shigenori Inoue[1], Keisuke Arimoto[1], Junji Yamanaka[1], Kiyokazu Nakagawa[1], Kentarou Sawano[2], Yasuhiro Shiraki[2], Atsushi Moriya[3], Yasuhiro Inokuchi[3] and Yasuo Kunii[3],
[1]Center for Crystal Science and Technology, University of Yamanashi, Japan,
[2]Research Center for Silicon Nano-Science, Musashi Institute of Technology, Japan,
[3]Hitachi Kokusai Electric Inc., Japan

10:20-10:24 P-06:
"Diffusion of Arsenic through Strained Si /Relaxed $Si_{1-x}Ge_x$ Heterostructure", ・・・ 33
Takamichi Sumitomo and Satoru Matsumoto,
Department of Electronics and Electrical Engineering, Keio University, Japan

10:24-10:28 P-07:
"Atomic Layer Doping of Phosphorus and Arsenic: Experimental and Atomistic Modeling", ・・・ 35
S. Takeuchi, L. Yang, N. D. Nguyen, R. Loo, T. Conard, G. Pourtois,
W. Vandervorst and M. Caymax,
IMEC, Belgium

10:28-10:32 P-08:
"Formation of Ultra High Density Si-based Quantum Dots on Ultrathin SiO_2", ・・・ 37
K. Makihara, A. Kawanami, M. Ikeda, S. Higashi and S. Miyazaki,
Graduate School of Advanced Sciences of Matter, Hiroshima University, Japan

10:32-10:36 P-09:
"AFM/KFM Detection of Si-tagged ProteinA on HF-last Si(100), Thermally Grown SiO_2 and Si-QDs Surfaces", ・・・ 39
K. Makihara, M. Ikeda, S. Higashi, Y. Hata, A. Kuroda and S. Miyazaki,
Graduate School of Advanced Sciences of Matter, Hiroshima University, Japan

10:36-10:40 P-10:
"Application of Relaxed Ge/Si(100) by ECR Plasma CVD to Highly Strained B Doped Si", ・・・ 41
Katsutoshi Sugawara, Masao Sakuraba and Junichi Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

10:40-10:44 P-11:
"P Atomic-Layer Doping in Heteroepitaxial Growth of Si on Strained $Si_{1-x}Ge_x$/Si(100) by Ultraclean Low-Pressure CVD", ・・・ 43
Yohei Chiba, Masao Sakuraba and Junichi Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

10:44-10:48 P-12:
"Formation of Nitrogen Atomic-Layer Doped Si/$Si_{1-x}Ge_x$/Si(100) Epitaxially Grown by Ultraclean Low-Pressure CVD", ・・・ 45
Tomoyuki Kawashima, Masao Sakuraba and Junichi Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

10:48-10:52 P-13:
"Epitaxial Growth of B Atomic-Layer Doped Si Film on Si(100) Using Electron-Cyclotron-Resonance Ar Plasma", ・・・ 47
Takayuki Nosaka, Masao Sakuraba and Junichi Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

10:52-10:56 P-14:
"Hole Resonant Tunneling Diodes Utilizing High Ge Fraction (x>0.5) Si/Strained $Si_{1-x}Ge_x$/Si(100) Heterostructure with Improved Performance at Higher Temperature above 200 K", ・・・ 49
Kuniaki Takahashi, Takahiro Seo, Masao Sakuraba and Junichi Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

10:56-11:00 P-15:
"Heat-Treatment Effect upon H-Terminated Structure Formed on Wet-Cleaned Si(100) and Ge(100)", ・・・ 51
Atsushi Uto[1], Masao Sakuraba[1], Matty Caymax[2] and Junichi Murota[1],
[1]Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan,
[2]IMEC, Belgium

Session V: Poster Presentation 11:00-12:00 (4F Room 401)

(Boards for posters are available during Workshop.)

12:00-13:05 **Lunch**

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Session VI: Regular Presentation (3) 13:05-15:10 (4F Conference Room)

13:05-13:25 Z-01:
"Formation of Metallic Nanodots on Ultrathin Gate Oxide Induced by H_2-plasma Treatment and Its Application to Floating Gate Memories", ・・・ 53
Seiichi Miyazaki, M. Ikeda, K. Makihara, K. Shimanoe and R. Matsumoto,
Graduate School of Advanced Sciences of Matter, Hiroshima University, Japan

13:25-13:30 **Session Introductory**
Junichi Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

13:30-13:50 Z-02:
"Transient Charge-Pumping Characteristics in SiGe/Si-Hetero-Channel MOSFETs", ・・・ 55
Toshiaki Tsuchiya[1], Keiichi Yoshida[1], Masao Sakuraba[2] and Junichi Murota[2],
[1]Interdisciplinary Faculty of Science and Engineering, Shimane Univ.,
[2] Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

13:50-14:10 Z-03:
"Ultra-low-power SiGe HBT Technology with Precisely Controlled Si/SiGe Epitaxial Growth", ・・・ 57
Makoto Miura[1], Katsuya Oda[1], Hiromi Shimamoto[2] and Katsuyoshi Washio[1],
[1]Central Research Laboratory, Hitachi, Ltd., Japan,
[2]Renesas Northern Japan Semiconductor, Inc., Japan

14:10-14:30 Z-04:
"A Ku-band Low Noise PLL using SiGe HBT ECL Phase Frequency Detector", ・・・ 59
Koji Tsutsumi, Masahiko Komaki and Noriharu Suematsu,
Mitsubishi Electric Corp., Japan

14:30-14:50 Z-05:
"Electrical Characterization and strain analysis with NBD method of Gate All Around (GAA) Strained-Silicon-On-Nothing (SSON) MOSFETs", ・・・ 61
Koji Usuda[1], S. Nakaharai[1], T. Irisawa[1], Y. Moriyama[1], N. Hirashita[1], T. Tezuka[1],
Y. Yamashita[1], N. Taoka[1], O. Kiso[1], T. Yamamoto[1], N. Sugiyama[1] and S. Takagi[2,3],
[1]MIRAI-ASET, Japan, [2]MIRAI-ASRC, AIST, Japan, [3]The University of Tokyo, Japan

14:50-15:10 Z-06:
"Formation of Tensile-Strained Ge Layers on $Ge_{1-x}Sn_x$ Buffer Layers and Control of Strain and Dislocation Structures", ・・・ 63
Osamu Nakatsuka[1], Yosuke Shimura[1], Akira Sakai[2] and Shigeaki Zaima[1],
[1]Graduate School of Eng., Nagoya University, Japan,
[2]Graduate School of Eng. Sci., Osaka University, Japan

15:10-15:30 **Break**

WORKSHOP SCIENTIFIC PROGRAM (Tentative)
September 27 (Saturday), 2008

Session VII: Regular Presentation (4) 15:30-17:30 (4F Conference Room)

15:30-15:50 Z-07:
"Indentation-Induced Solid-Phase Crystallization of SiGe on Insulator", ・・・ 65
Kaoru Toko, T. Sadoh and M. Miyao,
Department of Electronics, Kyushu University, Japan

15:50-16:10 Z-08:
"Fabrication of Advanced TiO_2/HfSiO/SiO_2 Layered Higher-*k* Dielectrics by Atomically Controlled In-situ PVD-Based Method", ・・・ 67
Heiji Watanabe[1], Hiroaki Arimura[1], Naomu Kitano[1, 2], Yuichi Naitou[3], Yudai Oku[1], Nobuo Yamaguchi[2], Motomu Kosuda[2], Takuji Hosoi[1] and Takayoshi Shimura[1],
[1]Department of Material and Life Science, Graduate School of Engineering, Osaka University, Japan,
[2]Electronic Devices Engineering Headquarters, Canon ANELVA Corporation, Japan,
[3]Nanoelectronics Research Institute, National Institute of Advanced Science and Technology, Japan

16:10-16:30 Z-09:
"Reaction kinetics on SiO_2 atomic layer deposition with tris-dimethyl aminosilane and ozone", ・・・ 69
Fumihiko Hirose[1],Yuta Kinoshita[1], Hironobu Miya[2], Kazuhiro Hirahara[3], Yasuo Kimura[4] and Michio Niwano[4],
[1]Graduate School of Sci. and Eng., Yamagata University, Japan,
[2]Hitachi Kokusai Electric Inc., Japan, [3]Shin-Etsu Chemical Co., Ltd., Japan,
[4]Res. Inst. Elec. Comm., Tohoku University, Japan

16:30-16:50 Z-10:
"Growth of 3C-SiC(111) on Si(110) substrate for graphene formation", ・・・ 71
Maki Suemitsu[1,2], Yu Miyamoto[1], Hiroyuki Handa[1] and Atsushi Konno[1],
[1]Research Institute of Electrical Communication, Tohoku University, Japan,
[2]CREST, Japan Science and Technology Agency, Japan

16:50-17:10 Z-11:
"$Si_{1-x}Ge_x$ Epitaxy Techniques and Their Application to Low Dimensional Devices", ・・・ 73
Yoshiyuki Suda, Hiroaki Hanafusa and Takafumi Okubo,
Graduate School of Engineering, Tokyo University of Agriculture and Technology, Japan

17:10-17:30 Z-12:
"Fabrication of Hole Resonant Tunneling Diodes Utilizing Nanometer-Order Strained SiGe/Si(100) Heterostructures with High Ge Fraction", ・・・ 75
Masao Sakuraba, Ryota Ito, Takahiro Seo and Junichi Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

17:30-17:40 **Closing Remarks**