Program

Sunday, June 2
(at Kofu Hotel)

17:30 – 20:30 Registration
19:00 – 20:30 Reception

Monday, June 3
(at Bellclassic Kofu)

Opening

9:00 – 9:10 Opening Address
Y. Shiraki
Department of Applied Physics, The University of Tokyo, Japan

Session I: Plenary Talks

9:10 – 9:40 I-01 Invited
Key Challenges in MIRAI Project
M. Hirose
Advanced Semiconductor Research Center, National Institute of Advanced Industrial Science and Technology, Japan

9:40 – 10:10 I-02 Invited
Si, SiGe, and Ge MOSFET Channels
E. A. Fitzgerald
Massachusetts Institute of Technology, USA

Coffee Break

Session II: Invited Talks (1)

10:30 – 11:00 II-01 Invited
A SiGe Base Heterojunction Bipolar Transistor by Using Self-Aligned Selective Epitaxial Growth Technique
F. Sato, T. Hashimoto, T. Yamazaki, and T. Tashiro
ULSI Device Development Div., NEC Corporation, Japan

11:00 – 11:30 II-02 Invited
Strain Relaxed Virtual Substrates – World Scene and New Developments.
T. J. Grasby, A Capewell and E.H.C. Parker
Semiconductor Research Group, Department of Physics, University of Warwick, UK

11:30 – 12:00 II-03 Invited
Phonon Engineering Based on Ge Isotope Superlattices
K. M. Itoh and K. Morita
Department of Applied Physics and Physico-Informatics, Keio University, Japan

Lunch Break

Session III: Optical Devices & Quantum Structures (Short Presentation)

13:30 – 13:33 III-01 Germanium Photodiodes Integrated on Silicon Substrates Using Nickel Germanide Contacts

G. Wöhl[1], C. Parry[1], E. Kasper[1], M.Jutzi[2] and M. Berroth[2]
[1]Institut für Halbleitertechnik, Universität Stuttgart, Germany
[2]Institut für Elektrische und Optische Nachrichtentechnik, Universität Stuttgart, Germany

13:33 – 13:36 III-02 Electroluminescence Properties of Si p-i-n Diode Structures with $Si/Si_{0.4}Ge_{0.6}$ Quantum Structures

K. Kawaguchi[1], K. Misawa[1], S. Koh[1] and Y. Shiraki[1], N. Usami[2]
[1]Department of Applied Physics, The University of Tokyo, Japan
[2]Institute for Materials Research (IMR), Tohoku University, Japan

13:36 – 13:39 III-03 SiGe Planar Microcavities With Strain-Balanced SiGe/Si Distributed Bragg Reflectors

K. Kawaguchi, K. Konishi, S. Koh, and Y. Shiraki
Department of Applied Physics, The University of Tokyo, Japan

13:39 – 13:42 III-04 Size Control of Dome-Shaped Ge Dot on Si(100) by Strain-Engineering

Y. Wakayama[1], L. V. Sokolov[2], N. Zakharov[3], P. Werner[3] and U. Gösele[3]
[1]National Institute for Materials Science, Nanomaterials Laboratory, Japan
[2]Institute of Semiconductor Physics, Russian Academy of Science, Novosibirsk, Russia
[3]Max-Planck Institute of Microstructure Physics, Germany

13:42 – 13:45 III-05 Photoluminescence of GeSi/Si(001) Self-Assembled Islands at Wavelengths up to 2 μm

A.V.Novikov, D.N.Lobanov, A.N.Yablonsky, Yu.N.Drozdov, N.V.Vostokov and Z.F.Krasilnik
Institute for Physics of Microstructures RAS, Russia

Session IV: Growth Technologies & Mechanisms (Short Presentation)

13:45 – 13:48 IV-01 Metal-Induced Crystallization of Amorphous SiGe Films on Insulator

H. Kanno[1], I. Tsunoda[1], A. Kenjo[1], T. Sadoh[1], S.

Yamaguchi[2], and M. Miyao[1]
[1]Department of Electronics, Kyushu University, Japan
[2]Central Research Lab., Hitachi Ltd., Japan

13:48 – 13:51 IV-02 Pre-Irradiation Effect on Solid-Phase Crystallization in a-$Si_{1-x}Ge_x$ on SiO_2
T. Sadoh[1], I. Tsunoda[1], A. Kenjo[1], S. Yamaguchi[2], and M. Miyao[1]
[1]Department of Electronics, Kyushu University, Japan
[2]Central Research Lab., Hitachi Ltd., Japan

13:51 – 13:54 IV-03 Effect of Ge on Solid Phase Epitaxy of $CoSi_2$ on Si(100)
O. Nakatsuka[1], H. Onoda[2], H. Ikeda[2], A. Sakai[2], S. Zaima[3], and Y. Yasuda[2]
[1]CIRSE, Nagoya University, Japan
[2]Dept. Crystal. Mat. Sci., Graduate School of Eng., Nagoya University, Japan
[3]CCRAST, Nagoya University, Japan

13:54 – 13:57 IV-04 Initial Adsorption of GeH_4 at Si Surfaces:
Separation between Chemistry and Strain
T. Murata, M. Suemitsu
R.I.E.C., Tohoku University, Japan

13:57 – 14:00 IV-05 Temperature-Programmed-Desorption Study on Surface Reactions of Organosilanes at Si(001)
K. Senthil[1], H. Nakazawa[2], M. Komatsu[3], T. Abe[4] and M. Suemitsu[1]
[1]R. I. E. C., Tohoku University, Japan
[2]Faculty of Science and Technology, Hirosaki University, Japan
[3]Tohoku Electric Power Co., Sendai, Japan
[4]Department of Electronics, Tohoku Institute of Technology, Japan

14:00 – 14:03 IV-06 High Quality Si Epitaxy by Sputtering Energy Control
H. Konta, T. Ikeda, K. Sasaki and T. Hata
Graduate School of Natural Science and Technology, Kanazawa University, Japan

14:03 – 14:06 IV-07 Fabrication of SiGe Substrate with Uniform Composition and its Application to Strain-Controlled Epitaxy of Group-IV Heterostructures
N. Usami[1], K. Kutsukake[1], Y. Azuma[1], K. Fujiwara[1], T. Ujihara[1], G. Sazaki[1], Y. Murakami[1], K. Nakajima[1], K. Nakagawa[2], and Y. Shiraki[3]
[1]Institute for Materials Research, Tohoku University, Japan
[2]Institute of Inorganic Synthesis, Yamanashi University, Japan
[3]Department of Applied Physics, School of

Engineering, The University of Tokyo, Japan

14:06 – 14:09 IV-08 Characteristics of Selective SiGe Growth on SOI Wafers

H. Choi, J. Shim, H. Oh, C. Lee, H. Kurino, M. Koyanagi
Dept. of Machine Intelligence and Systems Engineering, Tohoku University, Japan

14:09 – 14:12 IV-09 Surface Roughness of $Si_{1-x-y}Ge_xC_y$ Epitaxial Layers

I. Suzumura and K. Oda
Central Research Laboratory, Hitachi, Ltd., Japan

14:12 – 14:15 IV-10 Work Function of Impurity-Doped Poly-$Si_{1-x-y}Ge_xC_y$ Film Deposited by Ultraclean Low-Pressure CVD

H. Shim[1], M. Sakuraba[1], T. Tsuchiya[2], and J. Murota[1]
[1]Research Institute of Electrical Communication, Tohoku University, Japan.
[2]Interdisciplinary Faculty of Science and Engineering, Shimane University, Japan

14:15 – 14:18 IV-11 Dopant and Matrix Atom Segregation at Interfaces in Si / SiGe / Si Heterostructures: Characterization with High Depth Resolution

D. Krüger, D.Schmeißer, V. Melnik, R. Kurps, Y. Yamamoto, and B. Tillack
IHP, Germany

14:18 – 14:21 IV-12 Si Epitaxial Growth on SiH_3CH_3 Reacted Ge(100) and Intermixing between Si and Ge during Heat Treatment

K. Takahashi, M. Fujiu, M. Sakuraba and J. Murota
Research Institute of Electrical Communication, Tohoku University, Japan

Session V: Virtual Substrates (Short Presentation)

14:21 – 14:24 V-01 Control of Residual Strain in SiGe Buffer Layers on Si Substrates with Ultra-Thin Ge Interlayers

T. Yamamoto[1], T. Egawa[1], O. Nakatsuka[2], H. Ikeda[1], A. Sakai[1], S. Zaima[3] and Y. Yasuda[1]
[1]Department of Crystalline Materials Science, Graduate School of Engineering, Nagoya University, Japan
[2]CIRSE, Nagoya University, Japan
[3]CCRAST, Nagoya University, Japan

14:24 – 14:27 V-02 Surface Smoothing of Strain-Relaxed SiGe Layers on Si Substrates in Two-Step Strain-Relaxation Procedure

T. Egawa[1], T. Yamamoto[1], O. Nakatsuka[2], H. Ikeda[1], A. Sakai[1], S. Zaima[3], and Y. Yasuda[1]
[1]Department of Crystalline Materials Science, Graduate School of Engineering, Nagoya University,

Japan
[2]CIRSE, Nagoya University, Japan
[3]CCRAST, Nagoya University, Japan

14:27 – 14:30 V-03

H^+ Exposed $(Si_{14}/Ge_1)_{20}$ Superlattice Buffer for the Growth of $Si_{0.75}Ge_{0.25}$ Alloy Layers

M. M. Rahman, K. Kurumatani, T. Tambo and C. Tatsuyama
Department of Electrical and Electronic Engineering, Faculty of Engineering, Toyama University, Japan

14:30 – 14:33 V-04

Relaxation Enhancement of SiGe Thin Layers by Ion Implantation into Si Substrates

Y. Hirose[1], K. Sawano[2], S. Koh[2], K. Nakagawa[3], T. Hattori[1], and Y. Shiraki[2]
[1]Musashi Institute of Technology, Japan
[2]Department of Applied Physics, School of Engineering, The University of Tokyo, Japan
[3]Institute of Inorganic Synthesis, Yamanashi University, Japan

14:33 – 14:36 V-05

Fabrication of Ultrasmooth SiGe Virtual Substrates by CMP and their Application to Strained Si Modulation-Doped Structures

K. Sawano[1], K. Kawaguchi[1], Y. Hirose[2], S. Koh[1],K. Nakagawa[3], T. Hattori[2], and Y. Shiraki[1]
[1]Department of Applied Physics, School of Engineering, The University of Tokyo, Japan
[2]Musashi Institute of Technology, Japan
[3]Institute of Inorganic Synthesis, Yamanashi University, Japan

14:36 – 14:39 V-06

Evaluation of Dislocation Density in SiGe on Insulator Substrates by HF Defect

N. Sugiyama, Y. Moriyama, T. Tezuka, T. Mizuno, S. Nakaharai, K. Usuda, and S. Takagi
MIRAI Project, Association of Super-Advanced Electronics Technology, Japan

14:39 – 14:42 V-07

Fabrication of high-Ge Fraction Relaxed

SiGe-On-Insulator Virtual Substrate by Thermal Diffusion

A. Miura[1], T. Irisawa[1], S. Koh[1], K. Nakagawa[2], and Y. Shiraki[1]
[1]Department of Applied Physics, School of Engineering, The University of Tokyo, Japan
[2]Institute of Inorganic Synthesis, Yamanashi University, Japan

14:42 – 16:00 **Poster Session (III – V)**

(Coffee will be served.)

Session VI: Process Technologies (Short Presentation)

16:00 – 16:03 VI-01 Oxidation of Strained Si Layer Formed on $Si_{0.7}Ge_{0.3}$ Layer

M. Nakamura[1], M. Hara[1], J. Mitsui[1], Y. Hirose[1], K. Takahashi[1], H. Nohira[1], T. Hattori[1], K. Nakagawa[2] and Y. Shiraki[3]
[1]Musashi Institute of Technology, Japan
[2]Yamanashi University, Japan
[3]The University of Tokyo, Japan

16:03 – 16:06 VI-02 Heavy Boron Doping in Selective SiGe Growth by LPCVD

T. Udo[1], T. Hasimoto[2], T. Tominari[2], K. Tokunaga[2], Y. Kiyota[3]
[1]Hitachi ULSI Systems Co., Ltd.
[2]Device Development Center, Hitachi, Ltd.
[3]Central Research Laboratory, Hitachi, Ltd.

16:06 – 16:09 VI-03 Formation Mechanism of Low Resistance Contact in NiSi/Si System

O. Nakatsuka[1], Y. Tsuchiya[2], A. Sakai[2], S. Zaima[3] and Y. Yasuda[2]
[1]CIRSE, Nagoya University, Japan
[2]Dept. of Crystal. Mat. Sci., Graduate School of Eng., Nagoya University, Japan
[3]CCRAST, Nagoya University, Japan

16:09 – 16:12 VI-04 Structural and Electrical Properties in Ni/Si(100) Contacts

Y. Tsuchiya[1], O. Nakatsuka[2], A. Sakai[1], S. Zaima[2], and Y. Yasuda[1]
[1]Graduate School of Engineering, Nagoya University, Japan
[2]Center of Cooperative Research in Advanced Science and Technology, Nagoya University, Japan

16:12 – 16:15 VI-05 Side-Wall Protection by B in Poly-Si and $Si_{1-x}Ge_x$ in Gate Etching

H. Cho, T. Seino, A. Fukuchi, M. Sakuraba and J. Murota
Laboratory for Electronic Intelligent Systems, Research Institute of Electrical Communication, Tohoku University, Japan

16:15 – 16:18 VI-06 The effect of Ar^+ Ion Bombardment on Crystalline Quality of GeC/Si (001)

M. Okinaka, K. Miyatake, T. Tokuda, J. Ohta and M. Nunoshita
Graduate School of Materials Science, Nara Institute of Science and Technology, Japan

16:18 – 16:21	VI-07	Contact Resistivity between W and Heavily Doped $Si_{1-x-y}Ge_xC_y$ Epitaxial Film J. Noh[1], M. Sakuraba[1], J. Murota[1], S. Zaima[2] and Y. Yasuda[3] [1]Research Institute of Electrical Communication, Tohoku University, Japan [2]Center for Cooperative Research in Advanced Science and Technology, Nagoya University, Japan. [3]Graduate School of Engineering, Nagoya University, Japan
16:21 – 16:24	VI-08	Plasma Enhanced Processing of SiGe Wafers on a 300/200 mm Cluster Tool: Dry Cleaning combined with Epitaxy at Ultra-high Rates T. Buschbaum[1], H. M. Buschbeck[1], A. Erhart[1], Y. Göggel[1], J. Ramm[1], C. Rosenblad[1], S. Wiltsche[1], M. Kummer[2], H. von Känel[2], E. Müller[3], A. Dommann[4], T. Hackbarth[5], and G. Höck[5] [1]Unaxis Semiconductors, Principality of Liechtenstein [2]Laboratorium für Festkörperphysik, Switzerland [3]Laboratorium für Mikro- und Nanostrukturen, Switzerland [4]Interstate University of Applied Science Buchs, Switzerland [5]DaimlerChrysler Research and Technology, Germany
16:24 – 16:27	VI-09	Boron Atomic-Layer Doping in Low-Temperature Si Epitaxial Growth on Si(100) by Ultraclean Low-Pressure Chemical Vapor Deposition M. Nomura, M. Sakuraba and J. Murota Research Institute of Electrical Communication, Tohoku University, Japan
16:27 – 16:30	VI-10	Impact of a Controllable Base-Emitter Interfacial Oxide Layer on the SiGe HBT Device Properties J. Wen[1], K. Mutoh[2], P. Brabant[1] and J. Italiano[1] [1]ASM America Inc., USA [2]ASM Japan K.K, Japan
16:30 – 16:33	VI-11	Optimizing the Pre-Epitaxy Cleaning Regime for BiCMOS SiGe:C HBTs Y. Yamamoto, B. Tillack, D. Knoll and K. Köpke IHP, Germany
16:33 – 16:36	VI-12	Spectroscopic Ellipsometry for In-line Process Control of SiGe and SiGe:C HBT Film Stacks Y. Yamamoto[1], J. Bauer[1], P. Zaumseil[1], A. Goryachko[1], O. Fursenko[1], K. Köpke[1], B. Tillack[1] and T. Stoll[2] [1]IHP, Germany [2]KLA-Tencor GmbH, Germany

Session VII: Characterization & Transport Properties (Short Presentation)

16:36 – 16:39 VII-01

Evaluation of SiGe/Si Heterostructure Interface-Traps in SiGe-Channel MOSFETs

T. Tsuchiya[1], Y. Imada[1], and J. Murota[2]
[1]Interdisciplinary Faculty of Science and Engineering, Shimane University, Japan
[2]Research Institute of Electrical Communication, Tohoku University, Japan

16:39 – 16:42 VII-02

Ultra-High Effective Mobility in Strained Ge Channel p-Type Metal-Oxide-Semiconductor Field-Effect Transistors

T. Irisawa[1], S. Koh[1], K. Nakagawa[2] and Y. Shiraki[1]
[1]Department of Applied Physics, The University of Tokyo, Japan
[2]Institute of Inorganic Synthesis, Yamanashi University, Japan

16:42 – 16:45 VII-03

Irvin's Curves for B-Doped Relaxed $Si_{0.7}Ge_{0.3}$

S. Koh[1], K. Murata[1], T. Irisawa[1], Y. Shiraki[1] and K. Nakagawa[2]
[1]Department of Applied Physics, The University of Tokyo, Japan
[2]Institute of Inorganic Synthesis, Yamanashi University, Japan

Session VIII: Electronic Devices (Short Presentation)

16:45 – 16:48 VIII-01

Fabrication of Multi-Delta-Doped SiGe Channel p-MESFET

S. -C. Lee[1], S. –L. Wu[2], S. –J. Chang[1], A. Miura[3], S. Koh[3], and Y. Shiraki[3]
[1]Department of Electrical Engineering, National Cheng Kung University, Taiwan
[2]Department of Electronics Engineering, Cheng Shiu Institute of Technology, Taiwan
[3]Research Center for Advanced Science and Technology, University of Tokyo, Japan

16:48 – 16:51 VIII-02

Fabrication of Delta-Doped SiGe Channel p-MESFET Grown by MBE

P. –W. Chien[1], S. –L. Wu[2], S. –J. Chang[1], H. Miura[3], S. Koh[3], and Y. Shiraki[3]
[1]Department of Electrical Engineering, National Cheng Kung University, Taiwan
[2]Department of Electronics Engineering, Cheng Shiu Institute of Technology, Taiwan
[3]Research Center for Advanced Science and Technology, University of Tokyo, Japan

16:51 – 16:54 VIII-03 Electrical Properties of $Si_{1-x-y}Ge_xC_y$ Channel pMOSFET's
A. Inoue, T. Takagi, Y. Hara, Y. Kanzawa, H. Sorada, T. Kawashima and T. Ohnishi
Advanced Technology Research Laboratories, Matsushita Electric Industrial Co., Ltd., Japan

16:54 – 16:57 VIII-04 SiGe Channel p-MOSFETs with Schottky Source/Drain
K. Ikeda, Y. Yamashita, A. Endoh, T. Fukano, K. Hikosaka and T. Mimura
Fujitsu Laboratories Ltd., Japan

16:57 – 17:00 VIII-05 Fabrication of 0.1 μm SiGe-Channel pMOSFETs with In-Situ B-Doped SiGe Source/Drain
D. Lee[1], M. Sakuraba[1], J. Murota[1] and T. Tsuchiya[2]
[1]Laboratory for Electronic Intelligent Systems, Res. Inst. of Electr. Comm., Tohoku Univ., Japan
[2]Interdisciplinary Faculty of Science and Engineering, Shimane Univ., Japan

17:00 – 17:03 VIII-06 Double-Polysilicon Self-Aligned HBT with Non – Selective Epitaxial SiGe:C Base Layer
T. Yamazaki[1], S. Ohmi[1], M. Sakuraba[2], J. Murota[2], and T. Sakai[1]
[1]Department of Information Processing, Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology, Japan
[2]RIEC, Tohoku University, Japan

17:03 – 17:06 VIII-07 Application of SiGe to IGBT for High-Speed and Low-Loss Operation
T. Kudoh and T. Asano
Center for Microelectronic Systems, Kyushu Institute of Technology, Japan

17:06 – 18:30 Poster Session (V – VIII)

18:45 – 20:45 Banquet

Tuesday, June 4
(at Bellclassic Kofu)

Session IX: Invited talks (2)

9:00 – 9:30 IX-01 Mechanisms of Vertical Ordering in Stacked Layers of

	Invited	Self-Assembled Ge/Si(001) Quantum Dots V. Le Thanh Institut d'Electronique Fondamentale, Université Paris-Sud, France
9:30 – 10:00	IX-02 Invited	SiGe Optoelectronics L. Vescan Institut fuer Schichten und Grenzflaechen, Germany

Coffee Break

Session X: Invited talks (3)

10:30 – 11:00	X-01 Invited	Si-Ge HBT Application: Multi-10Gbit/s Interface Technologies for Optical Communications H. Ichino and Y. Miyamoto NTT Network Innovation Labs., Japan
11:00 – 11:30	X-02 Invited	Electron and Hole Mobility Improvement in Strained-Si MOSFETs by CMP N. Sugii, D. Hisamoto, K. Washio, N. Yokoyama, and S. Kimura Central Research Laboratory, Hitachi, Ltd., Japan
11:30 – 12:00	X-03 Invited	The Reaction of Substitutional Carbon with Silicon Self-Interstitials: Implications for Dopant Diffusion in Silicon Based Heterostructures M. S. Carroll[1], J. C. Sturm[2], T. Buyuklimanli[3], E. Napolitani[4], D. De Salvador[4], and M. Berti[4] [1]Agere Systems, USA [2]Princeton University, USA [3]Evans East, USA [4]INFM and Dept. of Physics, University of Padova, Italy
12:00 – 12:30	X-04 Invited	Novel Growth Method of Thin Strain-Relaxed SiGe Films on Si Substrates A. Sakai[1], K. Sugimoto[1], T. Yamamoto[1], M. Okada[1], H. Ikeda[1], O. Nakatsuka[2], S. Zaima[3], and Y. Yasuda[1] [1]Department of Crystalline Materials Science, Graduate School of Engineering, Nagoya University, Japan [2]CIRSE, Nagoya University, Japan [3]CCRAST, Nagoya University, Japan

Closing

12:30 – 12:40	Closing Remarks	Y. Yasuda Department of Crystalline Materials Science, Graduate School of Engineering, Nagoya University, Japan