5th International Workshop on New Group IV Semiconductor Nanoelectronics
Jan. 29(Fri.) - 30(Sat.), 2010
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., Sendai, Japan

Session 0: Opening  13:00-13:10 (4F Conference Room)

13:00-13:10  Introductory
Junichi Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

Session I: Invited Presentation (1)  13:10-14:50 (4F Conference Room)

13:10-13:35  I-01: “High frequency behaviour of Ge pin junctions”, Erich Kasper¹, M. Oehme¹, J. Schulze¹, S. Klinger² and M. Berroth²,
¹ Institut für Halbleitertechnik (IHT), Universität Stuttgart, Germany,
² Institut für Elektrische und Optische Nachrichtentechnik (INT), Universität Stuttgart, Germany

13:35-14:00  I-02: “Fluctuations in Electronic Properties of Interface Traps in Nano-MOSFETs”, Toshiaki Tsuchiya¹, Yuki Mori¹, Yuta Morimura¹ and Tohru Mogami²,
¹ Shimane University, Japan,
² Semiconductor Leading Edge Technologies (Selete), Japan

14:00-14:25  I-03: “Effective passivation of Ge surface by high-quality GeO₂ formed by Electron-Cyclotron-Resonance plasma oxidation for Ge-based electronic and photonic devices”, Yukio Fukuda¹, Yohei Otani¹, Tetsuya Sato², Hiroshi Toyota³ and Toshiro Ono³
¹ Tokyo University of Science, Suwa, Japan,
² Clean Energy Research Center, University of Yamanashi, Japan,
³ Hirosaki University, Japan

14:25-14:50  I-04: “Si₁₋ₓGeₓ GS-MBE and Sputter Epitaxy Techniques and Their Application to Devices with Low Dimensional Structures”, Yoshiyuki Suda, Hiroaki Hanafusa, Takafumi Okubo, Kouta Kunugi and Hiroyuki Ohhashi,
Graduate School of Engineering, Tokyo University of Agriculture and Technology, Japan

14:50-15:10 Break
Session II: Invited Presentation (2) 15:10-17:15 (4F Conference Room)

15:10-15:35  I-05: “Atomic Level Control for Group IV Semiconductor Processing”, Bernd Tillack\textsuperscript{1,2}, Yuji Yamamoto\textsuperscript{1} and Junichi Murota\textsuperscript{3},\textsuperscript{\textcopyright} IHP, Germany,\textsuperscript{\textcopyright} Technische Universität Berlin, Germany,\textsuperscript{\textcopyright} Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

15:35-16:00  I-06: “Germanium surface segregation in the silicon passivation of Ge pMOSFETs: influence of the Si precursor”, Matty Caymax, Benjamin Vincent, Wilfried Vandervorst and Roger Loo, IMEC, Belgium

16:00-16:25  I-07: “Defect Annihilation of \textit{a}-GeO\textsubscript{2} on Ge and Passivation of Ge/GeO\textsubscript{2} Interface”, Akira Toriumi, Department of Materials Engineering, The University of Tokyo, Japan

16:25-16:50  I-08: “Formation of graphene on 3C-SiC ultrathin film on Si substrates”, Maki Suemitsu\textsuperscript{1,2},\textsuperscript{\textcopyright} Research Institute of Electrical Communication, Tohoku University, Japan,\textsuperscript{\textcopyright} CREST, Japan Science and Technology Agency, Japan

16:50-17:15  I-09: “Si Single-Dopant FETs and Observation of Single-Dopant Potential by LT-KFM”, Michiharu Tabe\textsuperscript{1}, D. Moraru\textsuperscript{1}, M. Anwar\textsuperscript{1}, Y. Kawai\textsuperscript{1}, S. Miki\textsuperscript{1}, Y. Ono\textsuperscript{2} and T. Mizuno\textsuperscript{1},\textsuperscript{\textcopyright} Research Institute of Electronics, Shizuoka University, Japan,\textsuperscript{\textcopyright} NTT Basic Research Laboratories, Japan

Banquet 18:30-20:00 (Hotel Bel Air 1F)
Session III: Poster Presentation  9:30-11:30 (4F Room 401)

(Boards for posters are available during Workshop.)

P-01: “Interfacial Oxide Layer Controlled Al-Induced Crystallization of Si on Insulator for Epitaxial Template”, Masashi Kurosawa, Naoyuki Kawabata, Kaoru Toko, Taizoh Sadoh and Masanobu Miyao, Department of Electronics, Kyushu University, Japan

P-02: “Spin injection into Si channels through Fe3Si/Si Schottky tunnel barriers”, Kenji Kasahara1, Y. Ando1, Y. Enomoto2, K. Yamane1, K. Sawano2, K. Hamaya3 and M. Miyao1, 1 Department of Electronics, Kyushu University, Japan, 2 Department of Electrical and Electronic Engineering, Tokyo City University, Japan, 3 PRESTO, Japan Science and Technology Agency, Japan

P-03: “High-quality Co2FeSi/Si(111) heterointerfaces for spin injection into Si”, Shinya Yamada1, Y. Enomoto1, K. Kasahara1, T. Murakami1, K. Yamane1, K. Yamamoto1, Y. Ando1, K. Hamaya1,2 and M. Miyao1, 1 Department of Electronics, Kyushu University, Japan, 2 PRESTO, Japan Science and Technology Agency, Japan

P-04: “Adsorption and Desorption of Hydrogen on Si(100) in H2 or Ar Heat Treatment”, Atsushi Uto1, Masao Sakuraba1, Matty Caymax2 and Junichi Murota1, 1 Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan, 2 IMEC, Belgium

P-05: “Temperature-programmed-desorption study of graphene on silicon substrate”, Shunsuke Abe1, Hiroyuki Handa1, Yu Miyamoto1, Ryota Takahashi1, Hirokazu Fukidome1 and Maki Suemitsu2, 1 Research Institute of Electrical Communication, Tohoku University, Japan, 2 CREST, Japan Science and Technology Agency, Japan

P-06: “Effectiveness of (001) vicinal substrates on fabrication of high-quality diamond films using high-power-density microwave-plasma chemical-vapor-deposition method”, Osamu Maida, Shota Iguchi, Yasuhide Sunada, Teruhiro Hidaka and Toshimichi Ito, Graduate School of Engineering, Osaka University, Japan

P-07: “Carbon condensation and 3C-SiC growth caused by oxidizing Si1-xC0.5 alloy layers on Si(001) substrate”, Hideaki Hozumi1, S. Ogawa1, A. Yoshigoe2, S. Ishizuka3, J.R. Harries2, Y. Teraoka2 and Y. Takakuwa1, 1 Institute of Multidisciplinary Research for Advanced Materials, Tohoku University, Japan, 2 Quantum Beam Science Directorate, Japan Atomic Energy Agency, Japan, 3 Department of Applied Chemistry, Akita National College of Technology, Japan
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<th>Paper</th>
<th>Title</th>
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<td>P-08</td>
<td>“Microstructure Change of As-ion, B-ion, and Si-ion implanted Si&lt;sub&gt;0.99&lt;/sub&gt;C&lt;sub&gt;0.01&lt;/sub&gt; Thin Films by Thermal Annealing”</td>
<td>Shigenori Inoue&lt;sup&gt;1&lt;/sup&gt;, Keisuke Arimoto&lt;sup&gt;1&lt;/sup&gt;, Junji Yamanaka&lt;sup&gt;1&lt;/sup&gt;, Kiyokazu Nakagawa&lt;sup&gt;1&lt;/sup&gt;, Kentarou Sawano&lt;sup&gt;2&lt;/sup&gt;, Yasuhiro Shiraki&lt;sup&gt;3&lt;/sup&gt;, Atsushi Moriya&lt;sup&gt;3&lt;/sup&gt;, Yasuhiro Inokuchi&lt;sup&gt;2&lt;/sup&gt; and Yasuo Kunii&lt;sup&gt;3&lt;/sup&gt;, &lt;br&gt;&lt;sup&gt;1&lt;/sup&gt; Center for Crystal Science and Technology, University of Yamanashi, Japan, &lt;br&gt;&lt;sup&gt;2&lt;/sup&gt; Research Center for Silicon Nano-Science, Advanced Research Laboratories, Tokyo City University, Japan, &lt;br&gt;&lt;sup&gt;3&lt;/sup&gt; Hitachi Kokusai Electric Inc., Japan</td>
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<td>P-09</td>
<td>“Growth of SiGeC thin film on Si substrate by metal organic chemical vapor deposition”</td>
<td>Kouichi Kawasaki, S. Kitamura, Y. Naoi and S. Sakai, &lt;br&gt;Faculty of Engineering, The University of Tokushima, Japan</td>
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<td>P-10</td>
<td>“Microscopic characterization of Si(011)/Si(001) direct silicon bonding substrates”</td>
<td>Tetsuji Kato&lt;sup&gt;1&lt;/sup&gt;, T. Ueda&lt;sup&gt;1&lt;/sup&gt;, Y. Ohara&lt;sup&gt;1&lt;/sup&gt;, J. Kikkawa&lt;sup&gt;1&lt;/sup&gt;, Y. Nakamura&lt;sup&gt;1&lt;/sup&gt;, A. Sakai&lt;sup&gt;1&lt;/sup&gt;, O. Nakatsuka&lt;sup&gt;1&lt;/sup&gt;, S. Zaima&lt;sup&gt;2&lt;/sup&gt;, E. Toyoda&lt;sup&gt;3&lt;/sup&gt;, K. Izunome&lt;sup&gt;3&lt;/sup&gt;, Y. Imai&lt;sup&gt;4&lt;/sup&gt;, S. Kimura&lt;sup&gt;5&lt;/sup&gt; and O. Sakata&lt;sup&gt;4&lt;/sup&gt;, &lt;br&gt;&lt;sup&gt;1&lt;/sup&gt; Graduate School of Engineering Science, Osaka University, Japan, &lt;br&gt;&lt;sup&gt;2&lt;/sup&gt; Graduate School of Engineering, Nagoya University, Japan, &lt;br&gt;&lt;sup&gt;3&lt;/sup&gt; Covalent Materials Co., Ltd., Japan, &lt;br&gt;&lt;sup&gt;4&lt;/sup&gt; JASRI/SPring-8-8, Japan</td>
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<td>P-11</td>
<td>“Mobility Enhancement by Highly Strained Si on Relaxed Ge(100) Buffer Grown by Plasma CVD”</td>
<td>Katsutoshi Sugawara, Masao Sakuraba and Junichi Murota, &lt;br&gt;Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan</td>
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<td>P-12</td>
<td>“Control of Local Strain Structures by Microfabricated Shapes of Ge/Si&lt;sub&gt;1-x&lt;/sub&gt;Ge&lt;sub&gt;x&lt;/sub&gt; Layers”</td>
<td>Kenta Mochizuki, Takuya Mizutani, Osamu Nakatsuka, Hiroki Kondo and Sigeaki Zaima, &lt;br&gt;Graduate School of Engineering, Nagoya University, Japan</td>
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<td>P-13</td>
<td>“Strain Relaxation Behavior of Ge&lt;sub&gt;1-x&lt;/sub&gt;Sn&lt;sub&gt;x&lt;/sub&gt; Buffer Layers on Si and Virtual Ge Substrates”</td>
<td>Yosuke Shimura&lt;sup&gt;1&lt;/sup&gt;, Shotaro Takeuchi&lt;sup&gt;1&lt;/sup&gt;, Norimasa Tsutsui&lt;sup&gt;1&lt;/sup&gt;, Osamu Nakatsuka&lt;sup&gt;1&lt;/sup&gt;, Akira Sakai&lt;sup&gt;2&lt;/sup&gt; and Shigeaki Zaima&lt;sup&gt;1&lt;/sup&gt;, &lt;br&gt;&lt;sup&gt;1&lt;/sup&gt; Graduate School of Engineering, Nagoya University, Japan, &lt;br&gt;&lt;sup&gt;2&lt;/sup&gt; Graduate School of Engineering Science, Osaka University, Japan</td>
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<td>P-14</td>
<td>“Effective Mass and Mobility of Strained Ge (110) Inversion Layer for PMOSFET”</td>
<td>Wei-Ching Wang and Shu-Tong Chang, &lt;br&gt;Department of Electrical Engineering, National Chung Hsing University, Taiwan, R.O.C.</td>
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<td>P-15</td>
<td>“A Method of Selective Annealing of Ge Epitaxial Layers for Si-CMOS Backend Process”</td>
<td>Yu Horie, Yoichi Takada, Jiro Osaka, Yasuhiro Ishikawa and Kazumi Wada, &lt;br&gt;Department of Materials Engineering, The University of Tokyo, Japan</td>
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**P-16:** “Electronic States of Group IV Nanocompounds Probed by Soft X-ray Photoemission electron microscopy”, Hirokazu Fukidome¹, Arnold Alguno², Yu Miyamoto¹, Ryota Takahashi¹, Kei Imaizumi¹, Hiroyuki Handa¹, Yoshiharu Enta², Maki Sueyoshi¹, Masato Kotsugi¹, Takuo Ohkochi¹, Toyohiko Kinoshita¹ and Yoshihito Watanabe³, 
¹ Research Institute of Electrical Communication, Tohoku University, Japan, 
² Faculty of Science and Technology, Hirosaki University, Japan, 
³ JASRI/Spring-8, Japan

**P-17:** “Atomic Level Control of B doping in Ge”, Yuji Yamamoto¹, Rainer Kurps¹, Junichi Murota² and Bernd Tillack¹,³, ¹ IHP, Germany, ² Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan, ³ Technische Universität Berlin, Germany

**P-18:** “Vapor phase doping for ultra shallow junction formation in advanced Si CMOS devices”, Yasuo Shimizu¹,², N. D. Nguyen¹, S. Jiang¹, E. Rosseel¹, S. Takeuchi³, J.-L. Everaert¹, R. Loo¹, W. Vandervorst¹,³ and M. Caymax¹, ¹ IMEC, Belgium, ² Department of Applied Physics and Physico-Informatics, Keio University, Japan, ³ Department of Crystalline Materials Science, Nagoya University, Japan, ⁴ Department of Physics - IKS, KU Leuven, Belgium

**P-19:** “Heavy P Atomic-Layer Doping between Si and Si₀.₃Ge₀.₇(100) by Ultraclean Low Pressure CVD”, Yohei Chiba¹, Masao Sakuraba¹, Bernd Tillack²,³ and Junichi Murota¹, ¹ Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan, ² IHP, Germany, ³ Technische Universität Berlin, Germany

**P-20:** “Evaluation of Valence Band Offsets for SiO₂/Si/SiGe₀.₅/Si Heterostructures Using by X-ray Photoelectron Spectroscopy”, Akio Ohta¹, K. Makihara¹, S. Miyazaki¹, M. Sakuraba² and J. Murota², ¹ Graduate School of Advanced Sciences of Matter, Hiroshima University, Japan, ² Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

**P-21:** “Effect of Heavy Carbon Atomic-Layer Doping upon Intermixing and Strain at Si₁₋ₓGeₓ/Si(100) Heterointerface”, Tomoya Hirano¹, Masao Sakuraba¹, Bernd Tillack²,³ and Junichi Murota¹, ¹ Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan, ² IHP, Germany, ³ Technische Universität Berlin, Germany

**P-22:** “N Atomic-Layer Doping in Si/Si₁₋ₓGeₓ/Si(100) Heterostructure Growth By Low-Pressure CVD”, Tomoyuki Kawashima¹, Masao Sakuraba¹, Bernd Tillack²,³ and Junichi Murota¹, ¹ Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan, ² IHP, Germany, ³ Technische Universität Berlin, Germany
11:30-13:00  Lunch

**Session IV: Invited Presentation (3)  13:00-14:40 (4F Conference Room)**

13:00-13:25  I-10:  
“SiGe and GaAsP Metamorphic Systems: 1.9-2.3 eV III-V Band-GaP Integration on Si”,  
Eugene A. Fitzgerald, M.J. Mori, N. Yang and M.T. Bulsara,  
Department of Materials Science and Engineering, Massachusetts Institute of Technology (MIT), USA

13:25-13:50  I-11:  
“Effects of 193 nm Excimer laser radiation on SiO₂/Si/SiGe heterostructures grown on s-SOI substrates”,  
Stefano Chiussi¹, J.C. Conde¹, A. Benedetti², C. Serra², M. Sakuraba³ and J. Murota³,  
¹ Departamento de Física Aplicada, E.T.S.I.Industriales, Universidade de Vigo, Spain,  
² C.A.C.T.I., Universidade de Vigo, Spain,  
³ Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

13:50-14:15  I-12:  
“Potential of Ge₁₋ₓSnₓ alloys as high mobility channel materials and stressors”,  
Shotaro Takeuchi¹, Yosuke Shimura¹, Norimasa Tsutsui¹, Osamu Nakatsuka¹, Akira Sakai² and Shigeaki Zaima¹,  
¹ Graduate School of Engineering, Nagoya University, Japan,  
² Graduate School of Engineering Science, Osaka University, Japan

14:15-14:40  I-13:  
“Epitaxial Growth of Group IV Semiconductor Nanostructures Using Atomically Controlled Plasma Processing”,  
Masao Sakuraba, Takayuki Nosaka, Katsutoshi Sugawara and Junichi Murota,  
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, Japan

14:40-15:00  Break
Session V: Invited Presentation (4)  15:00-17:05 (4F Conference Room)

15:00-15:25 I-14:  
“Mn5Ge3/Ge heterostructures: perspectives for applications in spintronics and magnetic sensors”,  
Vinh Le Thanh, A. Spiesser, M.-T. Dau, L.A. Michez, J.-M. Raimondo, M. Petit, A. Glachant and J. Derrien,  
Centre Interdisciplinaire de Nanoscience de Marseille (CINaM)-CNRS, Aix-Marseille Université, France

15:25-15:50 I-15:  
“SiGe Mixing-Triggered Liquid-Phase Epitaxy for Defect-Free GOI (Ge on Insulator)”,  
Kaoru Toko, M. Kurosawa, T. Tanaka, T. Sadoh and M. Miyao,  
Department of Electronics, Kyushu University, Japan

15:50-16:15 I-16:  
“Fabrication method for triple coupled dots based on pattern-dependent oxidation”,  
Yasuo Takahashi¹, Mingyu Jo¹, Yuki Kato¹, Masashi Arita¹, Akira Fujiwara², Yukinori Ono², Katsuhiko Nishiguchi², Hiroshi Inokawa³ and Jung-Bum Choi⁴,  
¹ Graduate School of Information Science and Technology, Hokkaido University, Japan,  
² NTT Basic Research Labs., NTT Corporation, Japan,  
³ Research Inst. Electronics, Shizuoka University, Japan,  
⁴ Physics and Research Inst. NanoScience and Technology, Chungbuk National University, Korea

16:15-16:40 I-17:  
“Formation of Hybrid Nanodots Floating Gate for Functional Memories—Charge Storage Characteristics and Optical Response—”,  
Seiichi Miyazaki, N. Morisawa, S. Nakanishi, K. Makihera and M. Ikeda,  
Graduate School of Advanced Sciences of Matter, Hiroshima University, Japan

16:40-17:05 I-18:  
“High Mobility Ge CMOS Technologies”,  
Shinichi Takagi and Mitsuru Takenaka,  
Department of Electrical Engineering, The University of Tokyo, Japan

17:05-17:10 Closing Remarks