WORKSHOP SCIENTIFIC PROGRAM
Monday, October 2, 2006

Session 0: Opening Session 09:50-10:00

09:50-10:00 **Introductory**
Junichi Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., Japan

Session 1: Invited Session (1) 10:00-12:00 (4F Conference Room)

10:00-10:30 I-01: **"SiGe:C BiCMOS Technologies for High Frequency Applications"**,
Bernd Tillack, Bernd Heinemann, Dieter Knoll, Holger Rücker, Gerhard Fischer, Wolfgang Winkler, Wolfgang Mehr,
IHP, Germany

10:30-11:00 I-02: "**MMICs using SiGe BiCMOS**",
Katsuyoshi Washio, Nobuhiro Shiramizu, Toru Masuda,
Central Research Laboratory, Hitachi, Ltd., Japan

11:00-11:30 I-03: "**Mobility-Enhanced Device Technologies Using SiGe/Ge MOS Channels**",
Shinichi Takagi[1,2], T. Tezuka[3], T. Irisawa[3], S. Nakaharai[3], N. Hirashita[3], Y. Moriyama[3], K. Usuda[3], K. Ikeda[3], N. Taoka[3], Y. Yamashita[3], M. Harada[3], T. Maeda[1], T. Yamamoto[3] and N. Sugiyama[3],
[1]MIRAI-AIST, [2]Univ. Tokyo, [3]MIRAI-ASET, Japan

11:30-12:00 I-04: **"Strained Heterostructure p-MOSFETs"**,
Cait Ní Chléirigh, I. Åberg, G. Xia, J. L. Hoyt,
Microsystems Technology Laboratories, Department of Electrical Engineering and Computer Science, MIT, USA

12:00-13:20 **Lunch**

Session 2: Short Presentation (1) 13:20-14:20 (4F Conference Room)

13:20-13:24 P-01: "**Strain and Conductivity Behavior of Stripe Patterned Si/$Si_{1-x}Ge_x$/Si(100) Heterostructures**"
J. Uhm, M. Sakuraba, J. Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., Japan

13:24-13:28 P-02: "**Fabrication of Sub-100-nm Gate-Length SiGe-Heterochannel MOSFETs with In-Situ Doped Selectively Epitaxial SiGe Source/Drain**",
S. Takehiro[1], M. Sakuraba[1], T. Tsuchiya[2] J. Murota[1],
[1]Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., [2]Interdisciplinary Faculty of Science and Engineering, Shimane Univ., Japan

13:28-13:32 P-03: "**Mobility and 1/f Noise Dependence on In-plane Channel Direction of SiGe Channel PMOSFETs**",
Masato Toita, Tomohiko Chiaki,
Asahi Kasei Microsystems, Japan

13:32-13:36 P-04: "**Low Temperature Formation of SiGe/Glass Structures for System-in-Display Application**",
M. Miyao, H. Kanno, T. Sadoh,
Department of Electronics, Kyushu Univ., Japan

13:36-13:40 P-05: "**Formation of High Quality SiGe Virtual Substrate for Strained SOI Application**",
M. Tanaka, T. Sadoh, M. Miyao,
Department of Electronics, Kyushu Univ., Japan

13:40-13:44 P-06: "**Gas-source MBE of 3C-SiC(111) on Si(110) substrate using organosilane**",
A. Konno[1], M. Suemitsu[1], Y. Narita[2], T. Ito[1], K. Yasui[3], H. Nakazawa[4], T. Endoh[5],
[1]Center for Interdisciplinary Research, Tohoku Univ., [2]Kyushu Institute of Technology, [3]Dept.Electrical Engineering, Nagaoka Univ. Technology, [4]Department of Materials Science and Technology, Hirosaki Univ., [5]Research Institute of Electrical and Communication, Tohoku Univ., Japan

13:44-13:48 P-07: "**Scanning-tunneling-microscope observation on initial oxidization at Si surfaces**",
Y. Takahashi[1], H. Togashi[1], A. Kato[1], H. Asaoka[2], A. Konno[1], M. Suemitsu[1], Y. Teraoka[2], A. Yoshigoe[2],
[1]Center for Interdisciplinary Research, Tohoku Univ., [2]Japan Atomic Energy Agency, Tokai, Japan

13:48-13:52 P-08: "**Oxygen uptake during ultraviolet-ozone oxidation of HF-treated Si(110) surfaces**",
S. Hasegawa[1], T. Nakano[1], K. Ohmura[2], H. Matsuzawa[2], S. Asami[3], M. Suemitsu[1],
[1]Center for Interdisciplinary Research, Tohoku Univ., [2]NEC-TOKIN, [3]Sendai National College of Technology, Japan

13:52-13:56 P-09: "**Low-Temperature Growth of Highly Crystallized Poly-Si Thin Films on polyethylene-terephthalate (PET)**",
M. Matsumoto[1], M. Suemitsu[1], T. Yara[2], S. Nakajima[2], T. Uehara[2], Y. Toyoshima[3], S. Itou[4],
[1]Center for Interdisciplinary Research, Tohoku Univ., [2]Sekisui Chemicals Co. Ltd., [3]Energy Technology Research Institute, AIST, [4]Institute for Materials Research, Tohoku Univ., Japan

13:56-14:00 P-10: "**Strain Relaxation of Strained-Si Layers on (001) $Si_{1-x}Ge_x$-on-Insulator Substrates due to Misfit Dislocations**",
N. Hirashita[1], Y. Moriyama[1], E. Toyoda[2], N. Sugiyama[1], S. Takagi[3],
[1]MIRAI-ASET, [2]Toshiba Ceramics Co., Ltd., [3]MIRAI-AIST, Japan

14:00-14:04 P-11: "**Reduction of dislocation density in SGOI structures by two step oxidation and condensation method**",
N. Sugiyama[1], S. Nakaharai[1], N. Hirashita[1], T. Tezuka[1], Y. Moriyama[1], K. Usuda[1], S. Takagi[2,3],
[1]MIRAI-ASET, [2]MIRAI-AIST, [3]Univ. Tokyo, Japan

14:04-14:08 P-12: "**Oxidation and Reduction of GeO_x/Ge and GeO_x/Si in O_2 and N_2 Annealing**",
H. Nomura, T. Takahashi, T. Nishimura, K. Kita, A. Toriumi,
Department of Materials Engineering, Univ. Tokyo, Japan

14:08-14:12 P-13: "**Ge MIS Characteristics with GeN_x and GeON Layers Nitrided by Atomic Nitrogen Irradiation**",
T. Takahashi, H. Nomura, T. Nishimura, K. Kita, A. Toriumi,
Department of Materials Engineering, Univ. Tokyo, Japan

14:12-14:16 P-14: "**Subtleties in the epitaxial growth of Ge/Si nanstructures revealed by Raman scattering in combination with stable isotopes tracing**",
O. Moutanabbir, S. Miyamoto, K. M. Itoh,
Department of Applied Physics and Physico-Informatics, Keio Univ., Japan

14:16-14:20 P-15: "**Current Voltage Characterization in MIM Capacitor with High-K Dielectric by the Nonlinear RC Decay Method**",
Jung-Hsiang Lee,
Department of Electronic Engineering, Ching Yun Univ., Taiwan. R.O.C.

14:20-14:50 **Break**

Session 3: Invited Session (2) 14:50-16:20 (4F Conference Room)

14:50-15:20 I-05: **"Ge MOSFETs and high k gate dielectrics: a happy marriage thanks to thin epitaxial Si layers"**,
Matty Caymax[1], F. Leys[1], A. Dimoulas[2], S. Van Elshocht[1], M. Houssa[3], A. Delabie[1], T. Conard[1], B. De Jaeger[1], B. Kaczer[1], R. Bonzom[1], D. Nelis[1], W. Vandervorst[1], R. Loo[1], M. Meuris[1], M. M. Heyns[1],
[1]IMEC, Belgium, [2]MBE Laboratory, Institute of Materials Science, NCSR DEMOKRITOS, [3]Deptm. Electrical Engineering, K.U. Leuven, Belgium

15:20-15:50 I-06: **"Interface Properties of Ge with High-k Dielectrics and Metals"**,
Akira Toriumi, Koji Kita, Tomonori Nishimura,
Department of Materials Engineering, Univ. Tokyo, Japan

15:50-16:20 I-07: **"Growth and application of Ge dots in DotFETs"**,
Olaf Kirfel, M. Oehme, K. Lyutovich, E. Kasper,
Institut für Halbleitertechnik, Univ. Stuttgart, Germany

16:20-16:30 **Break**

Session 4: Invited Session (3) 16:30-18:00 (4F Conference Room)

16:30-17:00 I-08: "**Si Photonics -On chip optical interconnection and beyond-**",
Kazumi Wada,
Department of Materials Engineering, Univ. Tokyo, Japan

17:00-17:30 I-09: **"Si(Ge)- based structures and materials for spintronic applications: from MRAM to ferromagnetic semiconductors"**,
Vinh Le Thanh, S. Olive-Mendez, L. Michez, J. Derrien,
CRMCN-CNRS, Univ. Méditerranée, Campus Luminy, France

17:30-18:00 I-10: "**Control of Electronic Charged States of Si-based Quantum Dots for Floating Gate Application**",
Seiichi Miyazaki, K. Makihara, M. Ikeda,
Graduate School of Advanced Sciences of Matter, Hiroshima Univ., Japan

Banquet : 19:00-21:00 (Hotel Bel Air 1F)

Session 5: Short Presentation (2) 08:45-09:41 (4F Conference Room)

08:45-08:49 P-16: "**B Atomic Layer Formation on $Si_{1-x}Ge_x$(100) by Ultraclean LPCVD System**"
K. Ishibashi, M. Sakuraba, J. Murota, Y. Inokuchi, Y. Kunii, H. Kurokawa,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., Japan

08:49-08:53 P-17: "**Highly Strained-Si/Relaxed-Ge Epitaxial Growth on Si(100) by ECR Plasma CVD and Evaluation of Thermal Stability**",
K. Sugawara, M. Sakuraba, J. Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., Japan

08:53-08:57 P-18: "**Super-Critically-Thick Strained Si/SiGe CMOS Technology with Selective-Epitaxial-Si Shallow-Trench Isolation**",
M. Miyamoto[1], N. Sugii[2], Y. Yoshida[1], Y. Hoshino[3], Y. Kimura[2], M. Kondo[3], K. Ohnishi[3],
[1]Micro Device Division, Hitachi, Ltd., [2]Central Research Laboratory, Hitachi, Ltd,
[3]Renesas Technology Corp., Japan

08:57-09:01 P-19: "**A robust design approach for optimization of SiGe selective epitaxial growth technique**",
S. Eguchi[1], I. Miyashita[1], S. Nagashima[2], R. Takada[1], Y. Kagotoshi[1], H. Toyoda[2], A. Kanai[1], N. Machida[1],
[1]Renesas Technology Corp., [2]Renesas Eastern Japan Semiconductors Inc., Japan

09:01-09:05 P-20: "**Band Engineering and Process Technologies in SiGe BiCMOS for Highly-Sensitive and High-Speed Communication LSIs**",
Makoto Miura[1], Hiromi Shimamoto[3], Reiko Hayami[1], Akihiro Kodama[3], Tatsuya Tominari[2], Takashi Hashimoto[2], Katsuyoshi Washio[1],
[1]Central Research Laboratory, Hitachi, Ltd., [2]Micro Device Division, Hitachi Ltd.,
[3]Renesas Northern Japan Semiconductor. Inc., Japan

09:05-09:09 P-21: "**Formation of Highly-Crystallized Ge:H Films from VHF Inductively-Coupled Plasma of GeH_4**",
T. Sakata, K. Makihara, S. Higashi, S. Miyazaki,
Graduate School of Advanced Sciences of Matter, Hiroshima Univ., Japan

09:09-09:13 P-22: "**Characterization of Chemical Bonding Features of Silicon Oxynitride Films Formed on Ge(100) Surface**",
H. Nakagawa, A. Ohta, H. Murakami, S. Higashi, S. Miyazaki,
Graduate School of Advanced Sciences of Matter, Hiroshima Univ., Japan

09:13-09:17 P-23: "**Semiconductor Diode Laser Annealing of Amorphous Ge Films**",
K. Sakaike, S. Higashi, H. Kaku, T. Sakata, H. Murakami, S. Miyazaki,
Graduate School of Advanced Sciences of Matter, Hiroshima Univ., Japan

09:17-09:21 P-24: "**The hole density dependence of hole mobility in compressively strained Ge channel modulation-doped structures**",
K. Sawano[1], Y. Kunishi[1], H. Satoh[1], K. Nakagawa[2], Y. Shiraki[1],
[1]Research Center for Silicon Nano-Science, Advanced Research Laboratories, Musashi Inst. Technology, [2]Center for Crystal Science and Technology, Musashi Inst.Technology, Japan

09:21-09:25 P-25: "**Dislocation Structure and Strain Relaxation of SiGe and Ge Sub-micron Stripe Lines on Si(001) Substrates**",
O. Nakatsuka[1], S. Mochizuki[2], A. Sakai[2], H. Kondo[2], K. Yukawa[2], M. Ogawa[3], and S. Zaima[2],
[1]EcoTopia Science Institute, Nagoya Univ., [2]Department of Crystalline Materials Science, Graduate School of Engineering, Nagoya Univ., [3]Center for Cooperative Research in Advanced Science and Technology, Nagoya Univ., Japan

09:25-09:29 P-26: "**Mosaicity and Dislocations in Strain-Relaxed SiGe Buffer Layers on SOI Substrates**",
O. Nakatsuka[1], N. Taoka[2], A. Sakai[2], S. Mochizuki[2], M. Ogawa[3], S. Zaima[2],
[1]EcoTopia Science Institute, Nagoya Univ., [2]Department of Crystalline Materials Science, Graduate School of Engineering, Nagoya Univ., [3]Center for Cooperative Research in Advanced Science and Technology, Nagoya Univ., Japan

09:29-09:33 P-27: "**P atomic Layer Doping at Heterointerface of Epitaxial Si Layer and $Si_{1-x}Ge_x$(100) Substrate by Alternate Surface Reaction of PH_3 and Si_2H_6 in Ultraclean LPCVD**",
Y. Chiba, M. Sakuraba, J. Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., Japan

09:33-09:37 P-28: "**Thermal Stability of Nitrided Si Atomic Layer on Ge(100) Using Low Pressure CVD**"
N. Akiyama, M. Sakuraba, J. Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., Japan

09:37-09:41 P-29: "**Electrical Characteristics of Hole Resonant Tunneling Diodes with High Ge Fraction Si/Strained $Si_{1-x}Ge_x$ Heterostructures on Si(100) Grown by Low-Temperature Ultraclean LPCVD**",
T. Seo, M. Sakuraba, J. Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., Japan

09:41-10:00 **Break**

Session 6: Invited Session (3) 10:00-11:00 (4F Conference Room)

10:00-10:30 I-11: **"Formation of high quality SiGe buffers on Si and transport properties of structures grown on them"**,
Yasuhiro Shiraki,
Advanced Research Laboratories, Musashi Inst. Technology, Japan

10:30-11:00 I-12: "**Buffer layer technology with misfit dislocation engineering**",
Akira Sakai[1], Osamu Nakatsuka[2], Masaki Ogawa[3], Shigeaki Zaima[1],
[1]Graduate School of Engineering, Nagoya Univ., [2]EcoTopia Science Institute, Nagoya Univ., [3]Center for Cooperative Research in Advanced Science and Technology, Nagoya Univ., Japan

Session 7: Poster Presentation (P-01～P-29) 11:00-12:20 (5F Hallway)

(Boards for posters are available during Workshop.)

12:20-13:20 **Lunch**

Session 8: Regular Session (1) 13:20-15:10 (4F Conference Room)

13:20-13:30 "**Session Introductory**",
J. Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., Japan

13:30-13:50 O-01: "**Hot-Carrier-Degradation of Hetero-Interface in SiGe/Si-Hetero-MOSFETs**"
T. Tsuchiya[1], M. Sakuraba[2], J. Murota[2],
[1]Interdisciplinary Faculty of Science and Engineering, Shimane Univ., [2]Research Institute of Electrical Communication, Tohoku Univ., Japan

13:50-14:10 O-02: "**Design of intrinsic and extrinsic base process of SiGeC HBT**",
Yukihiro Kiyota[1], Hideo Yamagata[2]
[1]SONY Corp., [2]SONY Semiconductor Kyusyu., Japan

14:10-14:30 O-03: "**Low-Temperature Formation of Fe_3Si/SiGe Structures for Spintronics Application**",
T. Sadoh, K. Ueda, M. Kumano, M. Miyao,
Department of Electronics, Kyushu Univ., Japan

14:30-14:50 O-04: "**SiGe Sputter Epitaxy and Its Application to Quantum Effect Devices**",
Y. Suda, H. Hanabusa, T. Kobayashi, Y. Takahashi, H. Maekawa
Graduate School of Engineering, Tokyo Univ. Agriculture & Technology, Japan

14:50-15:10 O-05: "**Control of strain and dislocation structures in $Ge_{1-x}Sn_x$ buffer layers on virtual Ge substrates**",
S. Takeuchi[1], A. Sakai[1], O. Nakatsuka[2], M. Ogawa[3], S. Zaima[1],
[1]Graduate School of Engineering, Nagoya Univ., [2]EcoTopia Science Institute, Nagoya Univ., [3]Center for Cooperative Research in Advanced Science and Technology, Nagoya Univ., Japan

15:10-15:30 **Break**

Session 9: Regular Session (2) 15:10-17:20 (4F Conference Room)

15:30-15:50 O-06: "**Growth of high quality Ge epitaxial layer on Si(100) substrate using ultra thin $Si_{0.5}Ge_{0.5}$ buffer**",
J. Nakatsuru, H. Date, S. Mashiro, M. Ikemoto,
Canon ANELVA Corp., Japan

15:50-16:10 O-07: "**A Study on Low-Temperature Pre-Epi Surface Treatment Using Cl-based and Si-based Gas Mixture**",
J. Wang, K. Yamamoto, A. Moriya, Y. Hashiba, Y. Inokuchi, Y. Kunii,
Hitachi Kokusai Electric Inc., Japan

16:10-16:30 O-08: "**Initial oxidation of HF acid treated SiGe (100) surfaces**",
F. Hirose, M. Nagato, Y. Kinoshita,
Faculty of Engineering, Yamagata Univ., Japan

16:30-16:50 O-09: "**Epitaxial Growth of Group IV Semiconductor in ECR Plasma Enhanced CVD**",
M. Sakuraba, D. Muto, M Mori, K. Sugawara, J. Murota,
Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku Univ., Japan

16:50-17:10 O-10: "**Low-temperature formation of ultrathin SiC films on Si substrates and its application to ubiquitous devices**",
M. Suemitsu[1], A. Konno[1], Y. Narita[2], T. Ito[1], K. Yasui[3], H. Nakazawa[4], and T. Endoh[5],
[1]Center for Interdisciplinary Research, Tohoku Univ., [2]Kyushu Institute of Technology, [3]Department of Electrical Engineering, Nagaoka Univ. of Technology, [4]Department of Materials Science and Technology, Hirosaki Univ., [5]Research Institute of Electrical and Communication, Tohoku Univ., Japan

17:10-17:20 **Closing Remarks**