PROGRAM

Sunday, January 21

17:30-20:30 **Registration**

19:00-20:30 **Reception**

Monday, January 22

9:00-9:15 **Introductory Talk**

Special Session I : System Application of SiGe(C)

9:15-9:45 I-01 Invited
Technologies for Wireless: A Value-added Approach
A. Ourmazd
IHP, Germany

9:45-10:15 I-02 Invited
Self-Aligned SEG SiGe HBT and Bi CMOS Technology
K. Washio
ULSI Research Dept., Central Research Lab., Hitachi Ltd., Japan

10:15-10:45 I-03 Invited
SiGe Nanoelectronics: From Increasing CMOS Functionality to Quantum Information Systems Using Self-assembled Ge Quantum Dots on Si
K. L. Wang, J. L. Liu, and G. Jin
UCLA, USA

Session II : Electronic Devices & Fabrication (Short Presentation)

11:00-11:03 II-01
Low-Frequency-Noise and Its Correlation with Transconductance in $Si_{1-x}Ge_x$-Channel pMOSFETs
T. Tsuchiya, T. Matsuura*, and J. Murota*
Fac. of Interdisciplinary Science & Engineering, Shimane Univ., Japan
* RIEC, Tohoku Univ., Japan

11:03-11:06 II-02
High Hole Mobility in SiGe/Pure-Ge Channel /SiGe Hetero Structures and Its Application to FETs
S. Tokumitsu, T. Irisawa*, H. Miura*, S. Koh*, K. Nakagawa+, T. Hattori, and Y. Shiraki*
Dept. of Electrical & Electrical Engineering Musashi Inst. of Technology, Japan
* RCAST, Univ. of Tokyo, Japan
+ Inst. of Inorganic Synthesis, Yamanashi Univ., Japan

11:06-11:09 II-03 δ -Doped-Channel $Si_{1-x}Ge_x$ FETs Grown by MBE

H. Miura, Y. P. Wang*, S. Koh, S. L. Wu+, S. J. Chang*, and Y. Shiraki

RCAST, Univ. of Tokyo, Japan
* Dept. of Electrical Engineering, National Cheng Kung Univ., Taiwan
+ Dept. of Electronics Engineering, Cheng Shiu Inst. of Technology, Kaohsiung, Taiwan

11:09-11:12 II-04 Comparison of Temperature Dependent Device Parameters for Strained-$Si_{1-x}Ge_x$ and Partially Strain Compensated $Si_{1-x-y}Ge_xC_y$ Heterostructure PMOSFETs

S. K. Ray, G. S. Kar, S. Maikap, and S. K. Banerjee*

Dept. of Physics & Meteorology, IIT, India
* Microelectronics Research Center, Univ. of Texas, USA

11:12-11:15 II-05 High Performance SiGe Channel Heterostructure Dynamic Threshold pMOSFET (HDTMOS)

T. Takagi, A. Inoue, Y. Hara, Y. Kanzawa, and M. Kubo

Advanced Technology Research Laboratories, Matsushita Electric Industrial Co., Ltd., Japan

11:15-11:18 II-06 Si/SiGe-Heterojunction Bipolar Power Transistors for 25 V Cellular Base Station Type of Applications

T. Johansson, and W.-X. Ni*

Ericsson Microelectronics AB, Sweden
* Dept. of Physics, Linköping Univ., Sweden

11:18-11:21 II-07 Fabrication of 0.1µm MOSFETs with Super Self-Aligned Ultrashallow Junction Formed by Selective In-Situ Doped $Si_{1-x}Ge_x$ CVD

T. Yamashiro*, M. Sakuraba, T. Matsuura, J. Murota and T. Tsuchiya+

RIEC, Tohoku Univ., Japan

* Miyagi OKI Electric Co., Ltd., Japan

+ Fac. of Science and Engineering, Shimane Univ., Japan

11:21-11:24 II-08 Selective Growth of Amorphous SiGe Films for Facet-Free Elevated Source/Drain Structure

A. Miyauchi, Y. Inoue, and T. Andou*

Hitachi Research Lab., Hitachi Ltd., Japan
* Device Development Center, Hitachi Ltd., Japan

11:24-11:27 II-09 Ultra-Shallow Junction with Elevated SiGe Source/Drain Fabricated by Laser Induced Atomic Layer Doping

K.W. Koh, J.C. Bea, H. J. Oh, H. Choi, M.G. Lee, T. Tanabe, T. Hirosue, K. T. Park, H. Kurino, and M. Koyanagi

Dept. of Machine Intelligence & Systems Engineering, Tohoku Univ., Japan

11:27-11:30 II-10 Improvement of Thermal Stability in In-Situ Doped Poly-SiGe Gate on SiON

T. Sadoh, Fitrianto, A. Kenjo, A. Miyauchi*, H. Inoue*, and M. Miyao

Dept. of Electronics, Kyushu Univ., Japan
* Hitachi Research Lab., Hitachi., Japan

11:30-11:33 II-11 Etching Feature Improvement by Side-Wall Protection with B in P-Doped Polysilicon

A. Fukuchi, T. Seino, T. Matsuura and J. Murota

RIEC, Tohoku Univ., Japan

11:33-11:36 II-12 Heavy Doping Characteristics in Si Epitaxial Growth at 450°C by Alternate Supplies of PH_3 and SiH_4

Y. Shimamune, M. Sakuraba, T. Matsuura and J. Murota

RIEC, Tohoku Univ., Japan

11:36-11:39 II-13 Temperature Effects on Oxidization Process of SiGe-on-Insulator Structures to Form Thin and High-Ge-Content SiGe Virtual Substrates

N. Sugiyama, T. Tezuka, T. Mizuno, M. Suzuki*, Y. Ishikawa+, N. Shibata+, and S. Takagi

Advanced LSI Technology Lab., Corporate R&D Center, Toshiba Corp., Japan
* Environmental Engineering & Analysis Center, Corporate R&D Center, Toshiba Corp., Japan
+ Japan Fine Ceramics Center, Japan

11:39-11:42 II-14 Growth of $Si_{0.75}Ge_{0.25}$ Alloy Layers Using 1-Step Short-Period $(Si_{14}/Ge_1)_N$ Superlattices as Buffer Layers on Si(001) Substrates

M. M. Rahman, H. Matada, T. Tambo, and C. Tatsuyama

Dept. of Electrical & Electronic Engineering, Fac. of Engineering, Toyama Univ., Japan

11:42-11:45 II-15 Formation of Strain-Relaxed SiGe Films on Si Substrates with Cap Layers

K. Sugimoto, T. Yamamoto, M. Okada, H. Ikeda, A. Sakai, S. Zaima* and Y. Yasuda

Dept. of Crystalline Materials Science, Graduate School of Engineering, Nagoya Univ., Japan
* Center for Cooperative Research in Advanced Science & Technology, Nagoya Univ., Japan

11:45-11:48 II-16 Successful Fabrication of SiGe Bulk Crystal with Uniform Composition as a Substrate for Si-Based Heterostructures

Y. Azuma, N. Usami, T. Ujihara, G. Sazaki, Y. Murakami, K. Fujiwara, S. Miyashita*, and K. Nakajima

IMR, Tohoku Univ., Japan
* Toyama Medical & Pharmaceutical Univ., Japan

11:48-11:51 II-17 A Study from First Principles of Atomic and Electronic Structures in $Si_{1-x-y}Ge_xC_y$ Alloys

M. Ohfuti, Y. Sugiyama, Y. Awano, and N. Yokoyama

Fujitsu Laboratories Ltd., Japan

Special Session III : Process Technologies with SiGe(C)

14:00-14:30 III-01 Invited SiGe:C Epitaxy for HBT Applications

B. Tillack, D. Knoll, B. Heinemann, K. E. Ehwald, D. Wolansky, Y. Yamamoto, D. Krüger, and P. Schley

IHP, Germany

14:30-15:00 III-02 Invited Point Defect Engineering for Dopant Control in Silicon-Based Nanodevices

J.C. Sturm, M.S. Carroll, M. Yang*, E. Stewart, and J. Gray

Dept. of Electrical Engineering, Center for Photonics & Optoelectronic Materials, Princeton Univ., USA

15:00-15:30 III-03 Invited
Growth and Characterisation of Abrupt Doping Profiles in Si and SiGe Epitaxy
C.P. Parry, G. Eifler, M. Oehme, M. Bauer, E. Kasper, T. G. Grasby*, A. D. Lambert*
Inst. für Halbleitertechnik, Univ. Stuttgart, Germany
* Advanced. Semiconductor. Research. Group, Dept. of Physics, Univ. of Warwick, UK

15:30-16:00 III-04 Invited
$Si_{1-x}Ge_x$ Channel Field Effect Transistors Using δ -Doping Technique
S. J. Chang, and S. L. Wu*
Inst. of Microelectronics, Dept. of Electrical Engineering, National Cheng Kung Univ., Taiwan
* Dept. of Electronics Engineering, Cheng Shiu Inst. of Technology., Taiwan

Session IV : Growth Technologies & Materials (Short Presentation)

16:15-16:18 IV-01
Epitaxial Growth of $Si_{1-y}C_y$ Film by Low Temperature Chemical Vapor Deposition
S. Yagi, K. Abe, T. Okabayashi, A. Yamada, and M. Konagai
Dept. of Physical Electronics, Tokyo Inst. of Technology, Japan

16:18-16:21 IV-02
RTCVD of $Si_{1-x}Ge_x$:C in a Production Single Wafer Epitaxy System
D. J. Meyer
ASM America, Inc., USA

16:21-16:24 IV-03
Growth of High-Quality $Si_{1-x-y}Ge_xC_y$ Alloys over a Wide Range of Carbon Content Using Rapid Thermal Chemical Vapor Deposition
Y. Sakuma, T. Ueno, Y. Sugiyama, H. Tanaka, and N. Yokoyama
Fujitsu Laboratories Ltd., Japan

16:24-16:27 IV-04
Investigation of Epitaxy Loading and Geometry Effects in an 8-Inch SiGe:C BiCMOS Technology
D. Knoll, B. Heinemann, K.E. Ehwald, D. Wolansky, P. Schley, and B. Tillack
IHP, Germany

16:27-16:30 IV-05
Development of Ultraclean LPCVD Equipment for SiGe(C) Epitaxial Growth
Y. Kunii, Y. Inokuchi, A. Moriya, and J. Murota*
Hitachi Kokusai Electric Inc., Japan
* RIEC, Tohoku Univ., Japan

16:30-16:33 IV-06
Growth of $Si_{1-x-y}Ge_xC_y$ Crystals by UHV-CVD: Effect of Ge Content on Substitutional C Incorporation
Y. Kanzawa, K. Nozawa, T. Saitoh, T. Takagi and M. Kubo
Advanced Semiconductor Group, Advanced Technology Research Lab., Matsushita Electric. Industrial, Japan

16:33-16:36 IV-07
Properties of $Si_{1-x-y}Ge_xC_y$ Low-Temperature Epitaxial Growth by UHV/CVD
I. Suzumura, K. Oda, and K. Washio
Central Research Lab., Hitachi Ltd., Japan

16:36-16:39 IV-08
B- and P-Doped SiGe(C) Epitaxial Growth on Si(100) by Ultraclean LPCVD
T. Noda*, D. Lee, H. Shim, M. Sakuraba, T. Matsuura, and J. Murota
RIEC, Tohoku Univ., Japan

* Hitachi Kokusai Electric Co., Ltd., Japan

16:39-16:42 IV-09 Application of a Two-Step Growth to the Formation of Epitaxial $CoSi_2$ Films on Si(001) Surfaces

Y. Hayashi[*, +], T. Katoh, H. Ikeda, A. Sakai, S. Zaima[*], and Y. Yasuda

Dept. of Crystalline Materials Science, Graduate School of Engineering, Nagoya Univ., Japan
* Center for Cooperative Research in Advanced Science & Technology, Nagoya Univ., Japan
[+] Electronics & Information Dept., Nagoya Municipal Industrial Research Inst., Japan

16:42-16:45 IV-10 Effects of Sb Atoms on Epitaxial Growth of $CoSi_2$(100) Films on Si(100) Surfaces

H. Onoda[*], Y. Hayashi[*,#], H. Ikeda[*], A. Sakai[*], S. Zaima[+], and Y. Yasuda[*]

* Graduate School of Engineering, Nagoya Univ., Japan
[+] Center for Cooperative Research in Advanced Science & Technology, Nagoya Univ., Japan
[#] Electronics & Information Dept., Nagoya Municipal Industrial Research Inst., Japan

16:45-16:48 IV-11 First Principles Study on Heteroepitaxial $FeSi_2$ on Si(111)

K. Yamaguchi and K. Mizushima

Central Research Inst., Mitsubishi Materials Corp., Japan

16:48-16:51 IV-12 Solid-Phase Reactions of a Ti/$Si_{1-x}Ge_x$/Si System

A. Tobioka, A. Yamanaka, O. Nakatsuka, H. Ikeda, A. Sakai, S. Zaima[*] and Y. Yasuda

Graduate School of Engineering, Nagoya Univ., Japan
* Center for Cooperative Research in Advanced Science & Technology, Nagoya Univ., Japan

16:51-16:54 IV-13 Study on Solid-Phase Reactions in Ti/p^+-$Si_{1-x-y}Ge_xC_y$/Si(100) Contacts

A. Tobioka, Y. Tsuchiya, H. Ikeda, A. Sakai, S. Zaima[*], J. Murota[+], and Y. Yasuda

Graduate School of Engineering, Nagoya Univ., Japan
* Center for Cooperative Research in Advanced Science & Technology, Nagoya Univ., Japan
[+] RIEC, Tohoku Univ., Japan

17:00-18:30 **Poster Session II & IV** (II-01～II-17 & IV-01～IV-13)

18:45-20:45 **Banquet**

Tuesday, January 23

Special Session V : SiGe(C) Heterostructure Substrates for High Performance Devices

9:00-9:30	V-01 Invited	Application of Strained-Si Films and Strained-Si-on-Insulator Structures to Advanced CMOS S. Takagi, T. Mizuno, N. Sugiyama, T. Tezuka, T. Hatakeyama and A. Kurobe Advanced LSI Technology Lab., Corporate Research & Development Center, Toshiba Corp., Japan
9:30-10:00	V-02 Invited	High Ge Content SiGe MODFET Heterostructures on Virtual Substrates for Device Applications: HOLE MOBILITIES Higher than Electrons in the Room Temperature Range of Operation O. A. Mironov, M. Myronov, E. H. C. Parker, T. E. Whall Dept. of Physics, Univ. of Warwick, UK
10:00-10:30	V-03 Invited	SiGe Technology Reduced to Commercial Practice D. C. Houghton, S. Kovacic H. Lafontaine and N Rowell* SiGe Microsystems Inc, Canada * National Research Council, Canada

Session VI : Optical Devices, Quantum Dots & Quantum Effects (Short presentation)

10:45-10:48	VI-01	SiGe/Si Heterojunction Light Emitting Devices for Efficient Excitation of Er Ions, W.-X. Ni, C.-X. Du, A. Elfving, and G. V. Hansson Dept. of Physics, Linköping Univ., Sweden
10:48-10:51	VI-02	Electroluminescence Behavior of a Schottky-Type Asymmetric $Si_{1-x}Ge_x$/Si DQW Diode Y. Suda, S. Kaechi, and T. Date Fac. of Technology, Tokyo Univ. of Agriculture & Technology, Japan
10:51-10:54	VI-03	Surface Diffusion Limited Nucleation of Ge Dots on the Si(001) Surface Y. H. Wu, C. Y. Wang, Göran V. Hansson, and W.-X. Ni Dept. of Physics, Linköping Univ., Sweden
10:54-10:57	VI-04	$Si_{1-y}C_y$ Alloys Used as Self-Patterned Templates for Alignment of Ge Dots L. Simon, D. Aubel, G. Castelein*, M. Stoffel, J. L. Bischoff and L. Kubler Lab. de Physique et de Spectroscopie Electronique CNRS-ESA 7014, Fac. des Sciences et Techniques, Univ. de Haute Alsace, France * Inst. de Chimie des Surface et Interface CNRS UPR 9069, France
10:57-11:00	VI-05	Electro- and Photoluminescence of C-Induced Ge Quantum Dots A. Beyer, S. Stutz, H. Sigg, D. Grützmacher, M. Goryll*, T. Stoica*, L. Vescan* Lab. for Micro- & Nanotechnology, Paul-Scherrer-Inst., Switzerland * Inst. für Schicht- und Ionentechnik, Forschungszentrum Jürich, Germany

11:00-11:03 VI-06 Self-Ordering in Size and Position of Vertically Stacked Ge Islands

M. Miura, J. M. Hartmann*, J. Zhang*, S. Koh, B. A. Joyce*, and Y. Shiraki

RCAST, Univ. of Tokyo, Japan
* CEDM, Blackett Lab., Imperial College, UK

11:03-11:06 VI-07 Size Reduction of Ge Islands by Combining Vertical Stacking Effect and Low Temperature Growth

H. Takamiya, M. Miura*, J. Mitsui, S. Koh*, T. Hattori, and Y. Shiraki*

Dept. of Electrical & Electrical Engineering, Musashi Inst. of Technology, Japan
* RCAST, Univ. of Tokyo, Japan

11:06-11:09 VI-08 Strain-Balanced Si/$Si_{1-x}Ge_x$ Multiple Quantum Wells on $Si_{1-y}Ge_y$ Virtual Substrates for Optical Device Applications

K. Kawaguchi, S. Koh, Y. Shiraki, N. Usami*, J. Zhang+, N. J. Woods+, G. Breton+, and G. Parry+

RCAST, Univ. of Tokyo, Japan
* IMR, Tohoku Univ., Japan
+ CEMD, Imperial College, Blackett Lab., UK

11:09-11:12 VI-09 Growth and Characterisation of Si/SiGe Quantum Cascade Structures Deposited by Molecular Beam Epitaxy

G. Dehlinger, L. Diehl, U. Gennser, H. Sigg, E. Müller, S. Stutz, J. Faist*, K. Ensslin+, G. Bauer#, J. Stangl#, and D. Grützmacher

Lab. for Micro- & Nanotechnology, Paul-Scherrer-Inst., Switzerland
* Inst. of Physics, Univ. of Neuchâtel, Switzerland
+ Solid State Physics Lab., ETH Zürich, Switzerland
# Inst. für Halbleiterphysik, Johannes Kepler Univ. Linz, Austria

11:12-11:15 VI-10 Study of Influence of Si Growth Rate on Ge Surface Segregation by Si Knudsen Cell

K. Nakagawa, N. Sugii*, S. Yamaguchi+, and S. Park+

Inst. of Inorganic Synthesis, Yamanashi Univ., Japan
* Central Research Lab., Hitachi Ltd., Japan
+ Hitachi Research Lab., Hitachi Ltd., Japan

11:15-11:18 VI-11 Microscopic Analysis of Crystallization Process of Amorphous Si/Ge Multi-Layered Structures on Quartz Substrate

S. K. Park, S. Yamaguchi, and N. Sugii*

Hitachi Research Lab., Hitachi Ltd., Japan
* Central Research Lab., Hitachi Ltd., Japan

11:18-11:21 VI-12 Initial Growth Property of Ge on Si(100) Substrate by Ion-Beam Sputtering

K. Sasaki, and T. Hata

Graduate School of Natural Science & Technology, Kanazawa Univ., Japan

11:21-11:24 VI-13 Adsorption and Thermal Decomposition Processes of Silane on SiGe Surfaces

N. Kamakura, A. Seyama, M. Shinohara, Y. Kimura, and M. Niwano

RIEC, Tohoku Univ., Japan

11:24-11:27 VI-14 Suppressed Adsorption of Source-Gas Molecules on Strained Surface: RT Adsorption of GeH_4 on Ge(111)-5x5/Si(111)

T. Murata, M. Suemitsu, T. Abe*

RIEC, Tohoku Univ., Japan
* Dept. of Electronics, Tohoku Inst. of Technology, Japan

11:27-11:30 VI-15 Surface Chemistry During Si Gas-Source Molecular Beam Epitaxy In-Situ Doped with Phosphine

M. Suemitsu and Y. Tsukidate

RIEC, Tohoku Univ., Japan

11:30-11:33 VI-16 New Approach for Si Atomic-Layer-Controlled Growth Method Using Thermally-Cracked Hydride Molecule

N. Hosoya, S. Daiju, and Y. Suda

Fac. of Technology, Tokyo Univ. Agriculture & Technology, Japan

11:33-11:36 VI-17 Scanning Tunneling Microscopy Study of Ge Epitaxy on C-Adsorbed Si(100) Surfaces

Y. Torige, M. Okada, H.Ikeda, A. Sakai, S. Zaima* and Y. Yasuda

Dept. of Crystalline Materials Science, Graduate School of Engineering, Nagoya Univ., Japan
* Center for Cooperative Research in Advanced Science & Technology, Nagoya Univ., Japan

11:36-11:39 VI-18 Atomic-Order Plasma Nitridation of Si under the Si Surface Cooling

T. Seino, T. Matsuura and J. Murota

RIEC, Tohoku Univ., Japan

11:39-11:42 VI-19 Self-Limiting Surface Reaction of SiH_4 and CH_3SiH_3 on Ge(100)

M. Fujiu, M. Sakuraba, T. Matsuura and J. Murota

RIEC, Tohoku Univ., Japan

11:42-11:45 VI-20 Thermal Nitridation of Ultrathin Silicon Dioxide Films at 750-850^{o}C in an NH_3 Environment

O. Jintsugawa, M. Sakuraba, T. Matsuura and J. Murota

RIEC, Tohoku Univ., Japan

11:45-11:48 VI-21 Buffered HF Etching Characteristics of $Si_{1-x-y}Ge_xC_y$ Epitaxial Films

S. Ishida*,+, Y. Hashiba*, M. Miyamoto+, T. Matsuura* and J. Murota*

* RIEC, Tohoku Univ., Japan

+ Morita Chemical Industries Co., Ltd., Japan

11:48-11:51 VI-22 Anomaly of Ge Diffusion in Si/SiO_2 Structure

S. Yamaguchi, S. K. Park, N. Sugii*, and K. Nakagawa+

Hitachi Research Lab., Hitachi Ltd., Japan
* Central Research Lab., Hitachi Ltd., Japan
+ Inst. of Inorganic Synthesis, Yamanashi Univ., Japan

11:51-11:54 VI-23 Segregation and Diffusion of Ge and P for the In Situ P-Doped $Si_{1-x}Ge_x/Si$

K.W. Koh, J.C. Bea, H.J. Oh, H. Choi, T. Tanabe, M.G. Lee, T. Hirosue, K. T. Park, H. Kurino, and M. Koyanagi

Dept. of Machine Intelligence & Systems Engineering, Tohoku Univ., Japan

11:54-11:57 VI-24 Ge Diffusion and Strain Relaxation During Annealing of the Strained-$Si/Si_{0.7}Ge_{0.3}$

N. Sugii

Central Research Lab., Hitachi Ltd., Japan

11:57-12:00 VI-25 Epitaxial Growth of Pure ^{30}Si Layers on a Natural Si(100) Substrate Using Enriched $^{30}SiH_4$

Y. Nakabayashi, T. Segawa, H. I. Osman, K. Saito, S. Matsumoto, J. Murota[*], K. Wada[+], and T. Abe[#]

Dept. of Electronics & Electrical Engineering, Keio Univ., Japan

* RIEC, Tohoku Univ., Japan

+ Dept. of Materials Science & Engineering, Massachusetts Inst. of Technology, USA

Isobe R&D Center, Shin-Etsu Handotai, Japan

12:00-12:03 VI-26 Novel Ellipsometry Technique to Measure Strain in $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ Thin Films

S. Mukerjee, S. Madhavi, and V. Venkataraman

Dept. of Physics, Indian Inst. of Science, India

13:30-15:00 **Poster Session VI** (VI-01～VI-26)

Special Session VII : Advanced Analysis & Future Devices

15:10-15:40 VII-01 Invited High Spatial Resolution X-Ray Techniques for Semiconductor Studies

S. Lagomarsino, S. Di Fonzo[*], W. Jark[*], C. Giannini[+], L. De Caro[+] and A. Cedola

IESS-CNR, Rome, Italy

* Sincrotrone Trieste, Trieste, Italy

+ PASTIS-CNRSM, Brindisi, Italy

15:40-16:10 VII-02 Invited Self-Assembled Si/Ge Quantum Dots: Formation, Ordering and Infrared Applications

K. Brunner

Walter Schottky Inst., TU Munich, Germany

16:10-16:40 VII-03 Invited Relationship between Graded Layer Structures and Defects in Silicon-Germanium Virtual Substrates

K. Mizushima, I. Shiono, K. Yamaguchi, and N. Muraki[*]

Central Research Inst., Mitsubishi Materials Corp., Japan

* Mitsubishi Materials Silicon Corp., Japan

16:40-16:50 **Closing Remarks**