CONFERENCE SCIENTIFIC PROGRAM

Tuesday, January 14

19:00 - 21:00 **Reception**

Wednesday, January 15

09:00 - 09:15 **Introductory** (Symposion : Room A)

Session I : Plenary Talks (Symposion : Room A)

09:15 - 09:50 **Challenges of High Germanium Content SiGe Structures**
Plenary - Erich Kasper (University of Stuttgart)

09:50 - 10:25 **The Revolution in SiGe: Impact on Device Electronics**
Plenary - David Harame (IBM)

10:25 - 10:45 **Break**

Session II : Invited Talks (1) (Symposion : Room A)

10:45 - 11:10 **Circuit Applications of High-Performance SiGe:C HBTs Integrated in BiCMOS Technology**
Invited - W. Winkler, J. Borngräber, B. Heinemann, H. Rücker, R. Barth, J. Bauer, D. Bolze, E. Bugiel, J. Drews, K.-E. Ehwald, T. Grabolla, U. Haak, W. Höppner, D. Knoll, D. Krüger, B. Kuck, R. Kurps, M.Marschmeyer, H. H. Richter, P. Schley, D. Schmidt, R. Scholz, B. Tillack, D. Wolansky, H.-E. Wulf, Y. Yamamoto and P. Zaumseil (IHP)

11:10 - 11:35 **Advanced SiGe HBT Technologies and Applications**
Invited - Katsuyoshi Washio (Hitachi, Ltd.)

11:35 - 12:00 **Strained Si MOSFETs on Bulk and SiGe-on-Insulator (SGOI) Substrates**
Invited - K. Rim, L. Shi, K. Chan, J. Chu, D. Boyd, K. Jenkins, J. Ott , D. Lacey, P. Mooney, M. Cobb, N. Klymko, F. Jamin, S. Koester, and T. Kanarsky (IBM)

12:00 - 12:25 **Microwave performances of silicon heterostructure-FETs**
Invited - F. Aniel[1], M. Enciso[1], P. Crozat[1], R. Adde[1], T. Hackbarth[2], J-H. Herzog[2], U. König[2]
((1)Paris-South University, (2)DaimlerChrysler Research Center)

12:25 - 13:45 **Lunch**

[Parallel Session]

Session III-A : MOSFET (Symposion : Room A)

13:45 - 14:00 **25nm Gate Length Strained Silicon CMOS** - Qi Xiang, Jung-Suk Goo, Haihong Wang,
Regular Yayoi Takamura, Bin Yu, James Pan, Ammar Nayfeh, Allison Holbrook, Farzad Arasnia, Eric Paton, Paul Bessser, Max Sidorov, Ercan Adem, Anthony Lochtefeld*, Glyn Braithwaite*, Matthew Currie*, Richard Hammond*, Mayank Bulsara*, Ming-Ren Lin
(Advanced Micro Devices, Inc.,*AmberWave Systems Corporation)

14:00 - 14:15 Regular — **Performance Enhancement in 70nm Channel Length Strained $Si_{0.9}Ge_{0.1}$ pMOSFETs** - Zhonghai Shi, David Onsongo, Raghaw Rai*, Srikanth B. Samavedam* and Sanjay K. Banerjee (The University of Texas at Austin, *Motorola (Digital DNA Laboratories, Dan Noble Center))

14:15 - 14:30 Regular — **Fabrication of 0.12-μm SiGe-Channel MOSFET Containing High Ge Fraction with Ultrashallow Source/Drain Formed by Selective B-Doped SiGe CVD** - Doohwan Lee, Shinobu Takehiro, Masao Sakuraba, Junichi Murota and Toshiaki Tsuchiya* (Tohoku University, *Shimane University)

14:30 - 14:45 Regular — **Fabrication of strained Ge channel p-MOSFET with extremely high mobility** - T. Irisawa, S. Koh, K. Nakagawa*, Y. Shiraki (The University of Tokyo, *Yamanashi University)

14:45 - 15:00 Regular — **Strained-SiGe Channel p-MOSFETs with Platinum-Germanosilicide Schottky Source/Drain** - Keiji Ikeda, Yoshimi Yamashita, Akira Endoh, Tetsu Fukano, Kohki Hikosaka, and Takashi Mimura (Fujitsu Laboratories)

15:00 - 15:15 Regular — **SiGe Elevated Source/Drain Structure and Nickel Silicide Contact Layer for sub 0.1μm MOSFET** - JeoungChill Shim, HyuckJae Oh, Hoon Choi, Takeshi Sakaguchi, Hiroyuki Kurino and Mitsumasa Koyanagi (Tohoku University)

15:15 - 15:30 Regular — **Low frequency noise suppression and DC characteristics enhancement in sub-μm metamorphic p-MOSFETs with strained $Si_{0.3}Ge_{0.7}$ channel grown by MBE** - M. Myronov, S. Durov, O.A. Mironov, E.H.C. Parker and T.E. Whall, T. Hackbarth*, G. Hock*, H.J. Herzog* and U. Konig* (University of Warwick, *DaimlerChrysler Research Center)

15:30 - 15:50 **Break**

Session IV-A : MOSFET (Symposion : Room A)

15:50 - 16:05 Regular — **Low-Frequency Noise Characteristics in Strained SiGe Channel pMOSFET** - Akira Asai, Junko Sato-Iwanaga, Akira Inoue, Yoshihiro Hara, Yoshihiko Kanzawa, Haruyuki Sorada, Takahiro Kawashima, Teruhito Ohnishi, Takeshi Takagi, and Minoru Kubo (Matsushita Electric Industrial Co., Ltd.)

16:05 - 16:09 Short — **High Performance Si/SiGe Heterostructure MOSFETs for Low power and Low Noise RF/Microwave Circuit Applications** - P. W. Li, W. M. Liao, C. C. Shih, T. S. Kuo, L. S. Lai*, Y. T. Tseng*, and M. J. Tsai* (National Central University, *ITRI)

16:09 - 16:13 Short — **A Proposal of Multi-Layer Channel MOSFET: The Application of Selective Etching for Si/SiGe Stacked Layers** - T. Sakai, S. Ohmi, D. Sasaki, M. Sakuraba* and J. Murota* (Tokyo Institute of Technology, *Tohoku University)

16:13 - 16:17 Short — **Low Frequency Noise and Hetero-Interface Traps in SiGe-Channel pMOSFETs** - Toshiaki Tsuchiya, Yuji Imada, and Junichi Murota* (Shimane University, *Tohoku University)

16:17 - 16:21 Short — **Investigation of the Leakage Current in $Si_{0.7}Ge_{0.3}$ pMOSFETs Fabricated by Selective Epitaxial Growth** - A. Inoue, H. Sorada, Y. Hara, K. Nozawa, A. Asai Y. Kanzawa and T. Takagi (Matsushita Electric Industrial Co., Ltd.)

16:21 - 16:25 Short — **Influence of roughness with long correlation length on the electron mobility of strained silicon devices** - Isao Kitagawa, Takuya Maruizumi, and Nobuyuki Sugii (Hitachi)

16:25 - 16:29 Short — **Electrical properties of $Si_{1-y}C_y/Si/SiO_2$ stacks for sub 50nm strained-channel nMOSFETs** - [1,2]F. Ducroquet, [1]T. Ernst, [1,2]O. Weber, [1]J.-M. Hartmann, [1]V. Loup, [3]P. Besson, [1]L. Brévard, [1]J.L. Di Maria, [1]S. Deleonibus ([1]CEA – LETI/DTS – CEA/GRE, [2]LPM, INSA-Lyon, [3]STMicroelectronics)

16:29 - 16:33 Short — **Analysis of carrier generation lifetime in strained-Si / SiGe heterojunction MOSFETs from capacitance transient** - L.K.Bera, Shajan Mathew, N.Balasubramanian, G. Braithwaite*, M.T. Currie*, F. Singaporewala*, J. Yap*, R. Hammond*, A. Lochtefeld*, M. T. Bulsara*, and E. A. Fitzgerald* (Institute of Microelectronics, *AmberWave Systems Corp.)

16:33 - 16:37 Short — **Minority Carrier Lifetime and Diffusion Length in $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ Heterolayers** - S. K. Samanta, G. K. Dalapati, S. Chatterjee and C. K. Maiti (IIT)

16:37 - 16:41 Short — **Electrical Properties of ZrO_2 Films on $Si_{1-x-y}Ge_xC_y$ Epitaxial Layers** - S. Chatterjee, G. K. Dalapati, S. K. Samanta, and C. K. Maiti (IIT)

16:41 - 16:45 Late News — **Low-voltage CMOS operation of SiGe Heterostructure DTMOS** - H. Sorada, A. Inoue, Y. Hara, K. Nozawa, A. Asai, T. Kawashima, K. Katayama, and T. Takagi (Matsushita Electric Industrial Co., Ltd)

16:45 - 17:20 **Break [Next : Poster Session (1)]**

[Parallel Session]

Session III-B : HBT and The Other Devices (Symposion : Room B)

13:45 - 14:00 Regular — **Avalanche Considerations in SiGe HBT Scaling** - Greg Freeman, Basanth Jagannathan, Jae-Sung Rieh (IBM Microelectronics)

14:00 - 14:15 Regular — **Emitter Resistance Improvement in High-Performance SiGe HBTs** - Alvin Joseph, Peter Geiss, Xuefeng Liu, Jeffrey Johnson, Kathy Schonenberg*, Ashima Chakravarti*, David Ahlgren*, and James Dunn (IBM)

14:15 - 14:30 Regular — **Self-Aligned Heavily-Boron-Doped SEG SiGe HBT** - Eiji Ohue[1], Yukihiro Kiyota[1], Takashi Hashimoto[1], Tsutomu Udo[2], Akihiro Kodama[3], Hiromi Shimamoto[3], Reiko Hayami[1] and Katsuyoshi Washio[1] ([1]Hitachi Ltd., [2]Hitachi ULSI Systems Co. Ltd., [3]Hitachi Device Engineering Co. Ltd.)

14:30 - 14:45 Regular — **Influence of the Extrinsic Base on the Base Current Kink in SiGe BJTs** - Alexei Sadovnikov, Tracey Krakowski, and Monir El-Diwany (National Semiconductor Corp.)

14:45 - 15:00 Regular — **Design and optimization of a 200 GHz SiGe HBT collector profile by TCAD.** - Andreas D. Stricker, Jeffrey B. Johnson, Greg Freeman, and Jae-Sung Rieh (IBM Microelectronics Division)

15:00 - 15:15 Regular — **Resonant tunneling in Si-SiGe superlattices on relaxed buffer substrates** - S. Tsujino, S. Mentese, L. Diehl, E. Muller, B. Haas, D. Bachli, S. Stutz, H. Sigg, D. Grutzmacher, J. Faist* (Paul Scherrer Institut, *University of Neuchatel)

15:15 - 15:50 **Break**

Session IV-B : HBT and The Other Devices (Symposion : Room B)

15:50 - 15:54 Short — **The Effect of C on Emitter-Base Design for a Single-Polysilicon SiGe:C HBT with an IDP Emitter** - Erik Haralson, Erdal Suvar, Gunnar Malm, Henry Radamson, Yong-Bin Wang, Mikael Östling (Royal Institute of Technology (KTH))

15:54 - 15:58 Short — **Characterization of leakage current for SiGeC heterojunction bipolar transistors with a selectively grown collector** - E. Suvar, E. Haralson, H. H. Radamson, Y.-B. Wang, B. G. Malm and M. Östling (Royal Institute of Technology (KTH))

15:58 - 16:02 Short — **ESD Characterization of SiGe HBT in 0.18-µm SiGe BiCMOS Process** - Shiao-Shien Chen, Tung-Yang Chen, Tien-Hao Tang, Shao-Chang Huang, Tsun-Lai Hsu, Hua-Chou Tseng, Jen-Kon Chen, and Chiu-Hsiang Chou* (United Microelectronics Corporation, *Providence University)

16:02 - 16:06 Short — **The optimal base design for SiGe heterojunction bipolar transistors with high f_T** - L.S. Lai, Y.H. Liu, C.S. Liang, Y.T. Tseng, Y.M. Shiu, P.S. Chen, S.C. Lu, C.W. Liu and M.-J. Tsai (ITRI)

16:06 - 16:10 Short — **Low frequency noise behavior of advanced SiGe HBT** - A.Rennane*, L.Bary*, G. Niu**, J.D. Cressler**, J. Joseph***, J.Graffeuil* and R. Plana* (*LAAS-CNRS, **Alabama Microelectronics Science and Technology Center, ***IBM Microelectronics)

16:10 - 16:14 Short — **Reliability properties of SiGe HBT** - A.Rennane*, L.Bary*, J.L.Roux **, J.Kuchenbecker **, J.Graffeuil* and R. Plana* (*LAAS-CNRS and Université Paul Sabatier, ** CNES)

16:14 - 16:18 Short — **Achieving a SiGe HBT Epitaxial Emitter with Novel LowThermal Budget Technique** - Paul Brabant, Jianqing Wen, Joe Italiano, Trevan Landin, Nyles Cody and Lee Haen (ASM America Inc.)

16:18 - 16:22 Short — **Evaluation of Compact Noise Modeling for Si/SiGe HBTs Based on Hierarchical Hydrodynamic Noise Simulation** - M. Bartels , B. Neinhüs , C. Jungemann , B. Meinerzhagen (Universität Bremen)

16:22 - 16:26 Short — **Comparison of State-of-the-Art Bipolar Compact Models for SiGe-HBTs** - A. Chakravorty, R. Garg, and C. K. Maiti (IIT)

16:26 - 16:30 Short — **A noise and power analysis of SiGE HBT's for RF applications** - J. Raoult*, J. Verdier*, F. Calmon*, P.J. Viverge**, C. Gontrand* (*Laboratoire de Physique de la Matiè re, **Centre de Génie Electrique de Lyon)

16:30 - 16:34 Short — **A Direct Extraction Feature for Scattering Parameters of SiGe-HBTs** - S. Wagner[1], V. Palankovski[1], T. Grasser[1], G. Röhrer[2], and S. Selberherr[1] ([1]TU Vienna, [2]AustriamicrosystemsAG)

16:34 - 16:38 Short — **60nm gate-length Si/SiGe HEMT** - A. Kasamatsu*, K. Kasai*, K. Hikosaka*, T. Matsui* and T. Mimura** (*Communications Research Laboratory, **Fujitsu Laboratories Ltd.)

16:38 - 16:42 Short — **SiGe virtual substrate HMOS transistor for analogue applications** - K. Michelakis, S. Despotopoulos, V. Gaspari, A. Vilches, K. Fobelets, C. Papavassiliou, C. Toumazou, J. Zhang (Imperial College)

16:42 - 16:46 Short — **Effect of temperature on the transfer characteristic of a 0.5µm-gate Si:SiGe depletion-mode n-MODFET** - V. Gaspari†, K. Fobelets, J.E. Velazquez-Perez*, R. Ferguson, K. Michelakis, S.Despotopoulos, and C. Papavassilliou (Imperial College London, *Universidad de Salamanca)

16:46 - 16:50 Short — **Influence of substrate thinning on the threshold voltage of Si:SiGe Heterojunction MOSFETs** - S.M. Li, K. Fobelets , J.E. Velazquez-Perez*, V. Gaspari, R. Ferguson, K. Michelakis, S. Despotopoulos, and C. Papavassilliou (Imperial College London, *Universidad de Salamanca)

16:50 - 16:54 Short — **Nonvolatile Memory based on Ge/Si Hetero-Nanocrystals** - H.G. Yang, Y. Shi, L. Pu, R. Zhang, B. Shen, P. Han, S.L. Gu, and Y.D. Zheng (Nanjing University)

16:54 - 16:58 Short — **Si/SiGe heterojunction collector for low loss operation of Trench IGBT** - Tsugutomo Kudoh and Tanemasa Asano (Kyushu Institute of Technology)

16:58 - 17:20 **Break [Next : Poster Session (1)]**

[End of Parallel Session]

17:20 - 18:40 **Session V : Poster Session (1)** (Symposion : Room C)
(see the page "xvi")

18:40 - 19:00 **Break**

19:00 - 21:00 **Banquet**

Thursday, January 16

Session VI : Invited Talks (2) (Symposion : Room A)

08:45 - 09:10 Invited — **High Performance RF Front End Circuits using SiGe:C BiCMOS + Copper Technologies**
- Glenn Watanabe, Jeff Ortiz, Rick Holbrook (Motorola)

09:10 - 09:35 Invited — **Numerical Simulation of Strained Si/SiGe Devices: The Hierarchical Approach**
- B. Meinerzhagen, C. Jungemann, B. Neinhüs, M. Bartels (Universität Bremen)

09:35 - 10:00 Invited — **Selective Epitaxial Growth of SiGe:C for High Speed HBTs**
- H. Schäfer, J. Böck, R. Stengl, H. Knapp, K. Aufinger, M. Wurzer, S. Boguth, M. Rest, R. Schreiter, and T.F. Meister (Infineon Technologies)

10:00 - 10:20 **Break**

Session VII : Invited Talks (3) (Symposion : Room A)

10:20 - 10:45 Invited — **Interfacial Reaction and Electrical Properties in Ni/Si and Ni/SiGe Contacts**
- S. Zaima[1], O. Nakatsuka[1], A. Sakai[1], J. Murota[2], and Y. Yasuda[1] ([1]Nagoya University, [2]Tohoku University)

10:45 - 11:10 Invited — **Avoiding loading effects and facet growth: key parameters to successful implementation of selective epitaxial SiGe deposition for HBT-BiCMOS and high-mobility hetero-channel pMOS devices**
- Roger Loo, and Matty Caymax (IMEC)

11:10 - 11:35 Invited — **Laterally controlled nucleation of Ge nano dots by in-situ focused ion beam surface modification**
- M. Kammler*, R. Hull*, and F.M. Ross+ (*University of Virginia, +IBM T.J. Watson Research Center)

11:35 -12:00 Invited — **Self assembled SiGe islands: 2µm photoluminescence emission and 3D composition profiles**
- U. Denker(a), M. Stoffel(a), H. Sigg(b), O. G. Schmidt(a) ((a) Max-Planck-Institute, (b) Paul Scherrer Institut)

12:00 - 13:20 **Lunch**

[Parallel Session]

Session VIII-A : Strain Control , Epitaxy and Impurity (Symposion : Room A)

13:20 - 13:35 Regular — **Development of a new type of SiGe thin strain relaxed buffer based on the incorporation of a carbon-containing layer** - Romain Delhougne, Philippe Meunier-Beillard*, Matty Caymax, Roger Loo, Wilfried Vandervorst (IMEC, *Philips Research Leuven)

13:35 - 13:50 Regular — **Thin strain relaxed SiGe buffer layers on Si and SOI wafers made by He^+ ion implantation and annealing** - S. Mantl[1], B. Holländer[1], N. Hüging[2], M. Luysberg[2], St. Lenk[1], S.M. Hoog[1], H.-J. Herzog[3], T. Hackbarth[3], R. Loo[4], M. Bauer[5] ([1-2]Research Centre Juelich, [3]DaimlerChrysler, [4]IMEC, [5]ASM Germany)

13:50 - 14:05 Regular — **Low temperature H_2 cleaning of Si surface for 0.18-um SiGe-BiCMOS base epitaxy** - T.Tominari, Y.Nonaka, K.Sakai, S.Wada, T.Saito, K.Tokunaga, T.Jimbo, T.Udo*, Y.Kiyota and T.Hashimoto (Hitachi,Ltd., *Hitachi ULSI Systems)

14:05 - 14:20 Regular — **N_2 as carrier gas: an alternative to H_2 for enhanced epitaxy of Si, SiGe and SiGe:C** - P. Meunier-Beillard*, M. Caymax**, K. Van Nieuwenhuysen**, G. Doumen**, B. Brijs**, M. Hopstaken†, L. Geenen** and W. Vandervorst** (*Philips Research Leuven, **IMEC, †Philips Research Laboratories)

14:20 - 14:35 Regular — **Selective Epitaxial Growth of Si and SiGe for MOS transistors** - J.-M. Hartmann, F. Bertin, G. Rolland, F. Laugier, M.N. Séméria, P. Besson and P. Gentile (CEA-DRT – LETI/DTS – CEA/GRE.)

14:35 - 14:50 Regular — **High Performance SiGe:C HBTs Using Atomic Layer Base Doping** - Bernd Tillack, Yuji Yamamoto, Dieter Knoll, Bernd Heinemann, Peter Schley, Biswanath Senapati and Dietmar Krüger (IHP)

14:50 - 15:05 Regular — **Enhanced intrinsic Arsenic diffusion in SiGe strained layers.** - A. Pakfar, P. Holliger*, C. Fellous, D. Dutartre. T. Schwartzmann and H. Jaouen. (STMicroelectronics, *CEA-Leti)

15:05 - 15:20 Regular — **On the mechanism of ion- implanted As diffusion in relaxed SiGe** - S. Eguchi, S. J. Rhee[1], D.L. Kwong[1], I. Åberg[2], and J.L. Hoyt [2] (Hitachi Ltd., [1]Univ. of Texas at Austin, [2]MIT)

15:20 - 15:40 **Break**

Session IX-A : Strain Control , Epitaxy and Impurity (Symposion : Room A)

15:40 - 15:44 Short — **Fabrication SiGe-on-insulator by rapid thermal annealing of Ge thin film on Si-on-insulator substrate** - K.Kutsukake, N.Usami, K.Fujiwara, T.Ujihara, G.Sazaki, B.P.Zhang *and K.Nakajima (Tohoku University, *The Institute of Physical and Chemical Research (RIKEN))

15:44 - 15:48 Short — **Formation of thin SiGe virtual substrates by ion implantation into Si substrates** - K. Sawano [a], Y. Hirose [b], S. Koh [a], K. Nakagawa [c], T. Hattori [b], and Y. Shiraki [a] ((a) The University of Tokyo, (b) Musashi Institute of Technology, (c) Yamanashi University)

15:48 - 15:52 Short — **Strain-relaxation mechanisms of SiGe layers formed by two-step growth on Si(001) substrates** - T. Egawa, T. Yamamoto, N. Taoka, O. Nakatsuka, A. Sakai, S. Zaima, and Y. Yasuda (Nagoya University)

15:52 - 15:56 Short — **Dislocation structures and strain-relaxation in SiGe buffer layers on Si (001) with thin Ge interlayer** - T. Yamamoto, T. Egawa, N. Taoka O. Nakatsuka, A. Sakai, S. Zaima and Y. Yasuda (Nagoya University)

15:56 - 16:00 Short — **Evaluation of relaxation of strained-Si layers on SiGe-On-Insulator (SGOI) structures after mesa isolation** - Koji Usuda, T.Mizuno, T.Tezuka, N.Sugiyama, Y.Moriyama, S.Nakaharai and S.Takagi (MIRAI Project, ASET)

16:00 - 16:04 Short — **Influence of SiGe interlayer on the initinal growth of $Si_{1-x-y}Ge_xC_y$ on Si(100)** - S. Ariyoshi, S. Takeuchi, O. Nakatsuka,* A. Sakai, S. Zaima,** and Y. Yasuda (Nagoya University)

16:04 - 16:08 Short — **Roughening mechanisms of tensily strained $Si_{1-x-y}Ge_xC_y$ films grown by UHV-CVD : a way to maximize substitutional C incorporation** - Cyril Calmes[1], Daniel Bouchier[1], Catherine Clerc[2], Yulin Zheng[3] ([1-2]Université Paris-Sud, [3]Université Paris VI et Paris VII)

16:08 - 16:12 Short — **Production-ready Dry Cleaning and Deposition Processes for Low-Temperature Si and SiGe Epitaxy** - Kummer, M. [a], Dommann, A.[a], Buschbaum T. [b], Buschbeck, H. M.[b], Erhart, A.[b], Goeggel, Y.[b], Rosenblad, C. [b], Wiltsche, S.[b], Ramm, J.[b] ((a) Interstate University of Applied Science, (b) Unaxis Semiconductors)

16:12 - 16:16 Short — **$Si_{1-x}Ge_x$/Si strained epitaxial layer grown by UV/UHV/CVD** - Huiyong Hu, Heming Zhang, Xianying Dai, *Kaicheng Li, Bin Shu, Yi Lv (Xidian University, *National Lab of Analog Ics)

16:16 - 16:20 Short — **Si/SiGe Selective Epitaxial Growth by a Single-wafer Cold-wall UHVCVD System** - Supika Mashiro, Hiroki Date, Junko Nakatsuru, Satoshi Hitomi, and Junro Sakai (Anelva Corporation)

16:20 - 16:24 Short — **Carbon incorporation study for SiGeC epitaxy optimization in RTCVD** - F. Deleglise, C. Fellous and D. Dutartre (STMicroelectronics)

16:24 - 16:28 Short — **Low Temperature, High Growth Rate Epitaxial Silicon and Silicon Germanium Alloy Films** - Michael A. Todd and K. Doran Weeks (ASM America)

16:28 - 16:32 Short — **Growth of high quality epitaxial $Si_{1-x-y}Ge_xC_y$ layers using chemical vapor deposition** - J. Hallstedt, E. Suvar, P. O. A. Persson*, L.Hultman* and H. H. Radamson (Royal Institute of Technology (KTH), *Linköpings Universitet)

16:32 - 16:36 Short — **Reduced Pressure Chemical Vapour Deposition of high C content Si / $Si_{1-y}C_y$ heterostructures for n-type MOS transistors** - J.-M. Hartmann, T. Ernst, V. Loup, F. Ducroquet, G. Rolland, P. Holliger, F. Laugier, D. Lafond, M.N. Séméria and S. Deleonibus (CEA-DRT – LETI/DTS – CEA/GRE.)

16:36 - 16:40 Short — **A new technique to fabricate Ultra-Shallow-Junctions, combining in-situ vapor HCl etching and in-situ doped epitaxial SiGe re-growth** - Roger Loo[1], Matty Caymax[1], Philippe Meunier-Beillard[2], Ivan Peytier[1], Stefan Kubicek[1], Peter Verheyen[1], Richard Lindsay[1], and Olivier Richard[1] ([1]IMEC, [2]Philips Research Leuven)

16:40 - 16:44 Short — **In-situ B doping of SiGe(C) using BCl_3 by hot-wall LPCVD** - Yasuo Kunii, Yasuhiro Inokuchi, Atsushi Moriya and Harushige Kurokawa ,Junichi Murota* (Hitachi Kokusai Electric Inc., *Tohoku University)

16:44 - 16:48 Short — **Low-Temperature Dopant Activation Technology Using Elevated Ge-S/D Structure** - Hideki Takeuchi, Pushkar Ranade and Tsu-Jae King (University of California at Berkeley)

16:48 - 16:52 Short — **Relationship between Total Impurity(B or P) and Carrier Concentrations in SiGe Epitaxial Film Produced by the Thermal Treatment** - Jintae Noh, Shinobu Takehiro, Masao Sakuraba and Junichi Murota. (Tohoku University)

16:52 - 16:56 Short — **Characterization of As^+-ion-implanted layers in strained-Si/SiGe/Si hetero-structures** - T. Ishida*,T. Inada**, N. Sugii*** and S.Irieda* (*Hosei University, **Hosei University Reserch Institute, ***Hitachi Ltd.)

16:56 - 17:00 Short — **Segregation of Boron to Polycrystalline and Single-crystal $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ Layers** - E. J. Stewart and J. C. Sturm (Princeton University)

17:00 - 17:04 Short — **High Resolution Depth Profiling of Dopants in SiGe on Si (001)** - N.L Rowell*, D.C. Houghton**, M. Ward***, and D. Webb*** (*National Research Council of Canada, **AIXTRON Inc., ***ATMI Corp.)

17:04 - 17:08 Late News — **Thin, strain relaxed $Si_{1-x}Ge_x$ buffer layers on Si(001) substrates with low defect density and surface roughness** - S.H. Christiansen, P.M. Mooney, J.O. Chu (IBM T.J. Watson Research Center)

17:08 - 17:25 **Break [Next : Poster Session (2)]**

[Parallel Session]

Session VIII-B : Process Tech., Quantum Dot and Optical Devices (Symposion : Room B)

13:20 - 13:35 Regular — **Reactive Ion Etching of $Si_{1-x}Ge_x$ Alloy with Hydrogen Bromide** - C. S. Wang, D. Y. Shu, C. M. Liu, and M.-J. Tsai (ITRI)

13:35 - 13:50 Regular — **Etching Characteristics of Impurity-Doped $Si_{1-x}Ge_x$ Epitaxial Films Using Electron-Cyclotron-Resonance Chlorine Plasma** - Hang-Sup Cho, Shinobu Takehiro, Masao Sakuraba and Junichi Murota. (Tohoku University)

13:50 - 14:05 Regular — **Ge dependent morphological change in poly-SiGe formed by Ni-mediated crystallization** - H. Kanno, I. Tsunoda, A. Kenjo, T. Sadoh, and M. Miyao (Kyushu University)

14:05 - 14:20 Regular — **Enhanced growth of amorphous interlayer in Ti thin films on strained Si/SiGe relaxed substrates** - H. C. Chen, S. W. Lee, S. L. Cheng, L. J. Chen, P. S. Chen* and C. W. Liu* (National Tsing Hua University, *ITRI)

14:20 - 14:35 Regular — **Selective epitaxial growth of Ge quantum dots on patterned Si(001) surfaces** - Lam. H. Nguyen*, V. Le Thanh, V. Yam, D. Débarre, M. Halbwax, D. Bouchier (Université Paris-Sud)

14:35 - 14:50 Regular — **Shape and composition change of Ge dots due to Si capping** - O. Kirfel[1], E. Mü ller[1], D. Grützmacher[1], K.Kern[2], A.Hesse[3], J. Stangl[3], V. Holý[3], G. Bauer[3] ([1]Paul Scherrer Institut, [2]École Polytechnique Fédérale de Lausanne, [3]University of Linz)

14:50 - 15:05 Regular — **Room Temperature 1.3 and 1.5 μm Electroluminescence from Si/Ge Quantum Dots (QDs)/Si Multi-layers** - Z.Pei, P.S.Chen, L.S.Lai, S.C. Lu , M.-J. Tsai, W. H. Chang*, W.Y. Chen*, A.T. Chou*, and T.M. Hsu* (ITRI, *National Central University)

15:05 - 15:20 Regular — **High Speed Lateral PIN Germanium-on-Silicon Photodetectors** - G. Dehlinger, J. D. Schaub, J. O. Chu, S. J. Koester, Q. C. Ouyang and A. Grill (IBM)

15:20 - 15:40 **Break**

Session IX-B : Process Tech., Quantum Dot and Optical Devices (Symposion : Room B)

15:40 - 15:55 Regular — **SiGe PIN photodetector for infrared optical fiber links operating at 1.25 Gbit/s** - M. Jutzi[1], M. Berroth[1], G. Wöhl[2], C. Parry[2], E. Kasper[2] (Univ. Stuttgart)

15:55 - 15:59 Short — **Enhanced crystal nucleation in a-SiGe/SiO_2 by ion-irradiation assisted annealing** - I. Tsunoda, A. Kenjo, T. Sadoh, and M. Miyao (Kyushu University)

15:59 - 16:03 Short — **Self-Organized Ge/Si Islands Grown by a Homemade UHV/CVD System** - Jinzhong YU, Changjun HUANG, Buwen CHENG, Yuhua ZUO, Liping LUO, Zhenglin LEI and Qiming WANG (Institute of Semiconductors, Chinese Academy of Sciences)

16:03 - 16:07 Short — **Kinetics of Ge quantum islands capping by silicon** - V. Yam, V. Le Thanh, D. Débarre and D. Bouchier (Université Paris-Sud)

16:07 - 16:11 Short — **Optical Properties of Stacked Ge/Si Quantum Dots with Different Spacer Thickness Grown by Chemical Vapor Deposition** - W. Y. Chen, W.-H. Chang, A. T. Chou, T. M. Hsu, P. S. Chen*, Zingway Pei* and L. S. Lai* (National Central University, *ITRI)

16:11 - 16:15 Short — **Novel composite Ge/Si/Ge quantum dots with high PL efficiency and improved uniformity** - P. S. Chen, S. W. Lee, Y. H. Peng, Z. Pei, M. –J. Tsai ,C. W. Liu (ITRI)

16:15 - 16:19 Short — **Improved quality of Ge quantum dots in Ge/Si stacked layers by pre-intermixing treatments** - S. W. Lee[1.2], P. S. Chen[2], Y. H. Peng[2], C. W. Liu[2] and L. J. Chen[1] ([1]National Tsing Hua University, [2]ITRI)

16:19 - 16:23 Short — **Influence of Thermal Annealing on Compositional Mixing and Crystallinity of Highly-Selective Grown Si Dots with Ge Core** - Yudi Darma, Hideki Murakami and Seiichi Miyazaki (Hiroshima University)

16:23 - 16:27 Short — **Synthesis of Ge nanowires using Au nanoparticles catalyst on alumina template** - Ye Zhizhen, Wu Guibin Huang Jingyun, CuiJiFeng, Zhao Binghui (Zhejiang University)

16:27 - 16:31 Short — **2×2 Electrooptical Switch with SOI Waveguide** - Jinzhong YU, Qingfeng YAN, Jinsong XIA, Zhongchao FAN, Zhangtao WANG, Shaowu CHEN (Institute of Semiconductors)

16:31 - 16:35 Short — **Long-wavelength SiGe/Si MQW Resonant-Cavity-Enhanced photodetectors (RCE-PD) for application in Optical Fiber Communication Network** - Qiming Wang, Cheng Li, Buwen Cheng, Qinqing Yang, Zhenglin Lei and Jinzhong Yu (Institute of Semiconductors)

16:35 - 16:39 Short — **Fabrication of Epitaxial SiGe Optical Waveguide Structures** - Yihwan Kim, Dean Berlin, and Arkadii Samoilov (Applied Materials Inc.)

16:39 - 16:43 Short — **Schottky Quantum Dots Infrared Photodetector with Far Infrared Response** - Y. H. Peng[1], Jen-Hsiang Lu[1], C. H. Kuan[1], C. W. Liu[1], Pang-Shiu Chen[2], Z. Pei[2], M.–J. Tsai[2], S. W. Lee[3], L. J. Chen[3], M. H. Ya[1], Y. F. Chen[1] ([1]National Taiwan University, [2]ITRI, [3]National Tsing Hua University)

16:43 - 16:47 Late News — **Coupling effect dependent on the thickness of the spacer layer between double layer of Ge quantum dots embedded in Si** - Yin Rao, Qi Gao, Zuimin Jiang and Fang Lu (Fudan University)

16:47 - 17:25 **Break [Next : Poster Session (2)]**

[End of Parallel Session]

17:25 - 19:00 **Session X : Poster Session (2)** (Symposion : Room C)
(see the page "xx")

Friday, January 17

Session XI : Invited Talks (4) (Symposion : Room A)

08:45 - 09:10 Invited — **SiGe-MMIC circuit techniques for 3G wireless terminals** - Noriharu Suematsu (Mitsubishi Electric Corp.)

09:10 - 09:35 Invited — **An Impedance Hopping Free 2GHz SiGe Step Gain Amplifier** - Mitsuru Tanabe (Matsushita Electric Industrial Co., Ltd.)

09:35 - 10:00 Invited — **DC- and RF-performance of a cost-effective SiGe technology** - V. Dudek, J. Berntgen, P. Maier, M. Tortschanoff, W. Kraus (ATMEL)

10:00 - 10:20 **Break**

[Parallel Session]

Session XII-A : New Technique (Symposion : Room A)

10:20 - 10:35 Regular — **Si Atomic Layer Epitaxy from Thermally Cracked Si_2H_6 (TCH-ALE) and the mechanisms of the adsorption process** - Yoshiyuki Suda and Kazushi Miki* (Tokyo University of Agriculture and Technology, *National Institute of Advanced Industrial Science and Technology)

10:35 - 10:50 Regular — **GeH_4 adsorption on Si(001) at room temperature: transfer of H atoms to Si sites and atomic exchange between Si and Ge** - Takeshi Murata, Maki Suemitsu (Tohoku University)

10:50 - 10:54 Short — **Si self-diffusion in heavily B-doped epitaxial silicon** - K. Toyonaga[1], S. Rahamah Bt Aid[1], Y. Nakabayashi[1], S. Matsumoto[1], M. Sakuraba[2], Y. Shimada[2], A. Hashiba[2], and J. Murota[2] ([1]Keio University, [2]Tohoku University)

10:54 - 10:58 Short — **Adsorption kinetics of dimethylsilane on Si(001)** - K.Senthil[1], H.Nakazawa[2] and M.Suemitsu[1] ([1]Tohoku University, [2]Hirosaki University)

10:58 - 11:02 Short — **Kinetics of Epitaxial Growth of Si and SiGe films on (110) Si Substrates** - N. Sugiyama, Y. Moriyama, S. Nakaharai, T. Tezuka, T. Mizuno and S. Takagi (MIRAI project, ASET)

11:02 - 11:06 Short — **Local atomic structure in Czochralski-grown $Ge_{1-x}Si_x$ bulk alloys** - I. Yonenaga, M. Sakurai, M. H. F. Sluiter and Y. Kawazoe (Tohoku University)

11:06 - 11:10 Short — **Epitaxial Growth of N Delta Doped Si Films on Si(100) by Alternately Supplied NH_3 and SiH_4** - Youngcheon Jeong, Masao Sakuraba and Junichi Murota (Tohoku University)

11:10 - 11:30 **Break [Next : Poster Session (3)]**

[Parallel Session]

Session XII-B : Circuit Technology (Symposion : Room B)

10:20 - 10:35 Regular — **Static Frequency Divider Circuit using Strained SiGe p-MODFETs** - D. V. Singh, S. J. Koester, J. O. Chu, K. A. Jenkins, P. M. Mooney, Q. C. Ouyang, N. Ruiz, J. A. Ott, D. Ralston*, M. Wetzel*, P. M. Asbeck*, V. V. Patel, and A. Grill (IBM Research Division, *University of California)

10:35 - 10:50 Regular — **SiGe based Low Noise Amplifier for WLAN applications** - J.Sadowy[1, 2], V.Le-Goascoz[2], I.Telliez[2], J.Graffeuil[1], E.Tournier[1], L. Escotte[1] and R. Plana[1]. ([1]LAAS-CNRS, [2]STMicroelectronics)

10:50 - 10:54 Short — **The Comparison of Isolation Technologies and Device Models on SiGe Bipolar Low Noise Amplifier** - W.-C. Hua[a], T.-Y. Yang[b], C. W. Liu[a,b] ([a]National Taiwan University, [b]STC/ITRI)

10:54 - 10:58 Short — **Design of a 4.4-5 GHz LNA in 0.25-µm SiGe BiCMOS Technology** - Paolo Crippa, Simone Orcioni, Francesco Ricciardi, and Claudio Turchetti (University of Ancona)

10:58 - 11:02 Short — **Design of a DC-5 GHz MOS-based SPDT T/R Switch in 0.25-µm SiGe BiCMOS Technology** - Paolo Crippa, Simone Orcioni, Francesco Ricciardi, and Claudio Turchetti (University of Ancona)

11:02 - 11:06 Short — **A 2.9GHz-Band SiGe-MMIC On-Chip VCO** - Yasuhiro Nabeno, Masayoshi Ono, Takayuki Sugano, Masahiko Nakanishi, Noriharu Suematsu (Mitsubishi Electric Corp.)

11:06 - 11:30 **Break [Next : Poster Session (3)]**

[End of Parallel Session]

11:30 - 12:30 **Session XIII : Poster Session (3)** (Symposion : Room C)
(see the page "xxiv")

12:30 - 13:45 **Lunch**

Session XIV : Invited Talks (5) (Symposion : Room A)

13:45 - 14:10 **Low-cost Circuit Solutions for Micro- and Millimeter Wave Systems using Commercially Available SiGe Technologies**
- Hermann Schumacher, Peter Abele, Ertugrul Sönmez, Kai-Boris Schad, and Andreas Trasser (University of Ulm)

14:10 - 14:35 **Optimization of SiGe HBTs for Industrial Applications**
- V. Palankovski and S. Selberherr (Institute for Microelectronics, TU Vienna)

14:35 - 15:00 **Fabrication and Device Characteristics of Strained-Si-On-Insulataor (Strained-SOI) CMOS**
- Shin-ichi Takagi, Tomohisa Mizuno, Tsutomu Tezuka, Naoharu Sugiyama, Toshinori Numata, Koji Usuda, Yoshihiko Moriyama, Shu Nakaharai, Junji Koga, Akihito Tanabe and Tatsuro Maeda* (MIRAI-Project, ASET, *National Institute of Advanced Industrial Science and Technology (AIST))

15:00 - 15:15 **Closing Session** (Symposion : Room A)

Poster Session (1)
17:20 - 18:40 Wednesday, January 15

MOSFET

P1-01 **25nm Gate Length Strained Silicon CMOS** - Qi Xiang, Jung-Suk Goo, Haihong Wang, Yayoi Takamura, Bin Yu, James Pan, Ammar Nayfeh, Allison Holbrook, Farzad Arasnia, Eric Paton, Paul Bessser, Max Sidorov, Ercan Adem, Anthony Lochtefeld*, Glyn Braithwaite*, Matthew Currie*, Richard Hammond*, Mayank Bulsara*, Ming-Ren Lin (Advanced Micro Devices, Inc.,*AmberWave Systems Corporation)

P1-02 **Performance Enhancement in 70nm Channel Length Strained $Si_{0.9}Ge_{0.1}$ pMOSFETs** - Zhonghai Shi, David Onsongo, Raghaw Rai*, Srikanth B. Samavedam* and Sanjay K. Banerjee (The University of Texas at Austin, *Motorola (Digital DNA Laboratories, Dan Noble Center))

P1-03 **Fabrication of 0.12-µm SiGe-Channel MOSFET Containing High Ge Fraction with Ultrashallow Source/Drain Formed by Selective B-Doped SiGe CVD** - Doohwan Lee, Shinobu Takehiro, Masao Sakuraba, Junichi Murota and Toshiaki Tsuchiya* (Tohoku University, *Shimane University)

P1-04 **Fabrication of strained Ge channel p-MOSFET with extremely high mobility** - T. Irisawa, S. Koh, K. Nakagawa*, Y. Shiraki (The University of Tokyo, *Yamanashi University)

P1-05 **Strained-SiGe Channel p-MOSFETs with Platinum-Germanosilicide Schottky Source/Drain** - Keiji Ikeda, Yoshimi Yamashita, Akira Endoh, Tetsu Fukano, Kohki Hikosaka, and Takashi Mimura (Fujitsu Laboratories)

P1-06 **SiGe Elevated Source/Drain Structure and Nickel Silicide Contact Layer for sub 0.1µm MOSFET** - JeoungChill Shim, HyuckJae Oh, Hoon Choi, Takeshi Sakaguchi, Hiroyuki Kurino and Mitsumasa Koyanagi (Tohoku University)

P1-07 **Low frequency noise suppression and DC characteristics enhancement in sub-µm metamorphic p-MOSFETs with strained $Si_{0.3}Ge_{0.7}$ channel grown by MBE** - M. Myronov, S. Durov, O.A. Mironov, E.H.C. Parker and T.E. Whall, T. Hackbarth*, G. Hock*, H.J. Herzog* and U. Konig* (University of Warwick, *DaimlerChrysler Research Center)

P1-08 **Low-Frequency Noise Characteristics in Strained SiGe Channel pMOSFET** - Akira Asai, Junko Sato-Iwanaga, Akira Inoue, Yoshihiro Hara, Yoshihiko Kanzawa, Haruyuki Sorada, Takahiro Kawashima, Teruhito Ohnishi, Takeshi Takagi, and Minoru Kubo (Matsushita Electric Industrial Co., Ltd.)

P1-09 **High Performance Si/SiGe Heterostructure MOSFETs for Low power and Low Noise RF/Microwave Circuit Applications** - P. W. Li, W. M. Liao, C. C. Shih, T. S. Kuo, L. S. Lai*, Y. T. Tseng*, and M. J. Tsai* (National Central University, *ITRI)

P1-10 **A Proposal of Multi-Layer Channel MOSFET: The Application of Selective Etching for Si/SiGe Stacked Layers** - T. Sakai, S. Ohmi, D. Sasaki, M. Sakuraba* and J. Murota* (Tokyo Institute of Technology, *Tohoku University)

P1-11 **Low Frequency Noise and Hetero-Interface Traps in SiGe-Channel pMOSFETs** - Toshiaki Tsuchiya, Yuji Imada, and Junichi Murota* (Shimane University, *Tohoku University)

P1-12 **Investigation of the Leakage Current in $Si_{0.7}Ge_{0.3}$ pMOSFETs Fabricated by Selective Epitaxial Growth** - A. Inoue, H. Sorada, Y. Hara, K. Nozawa, A. Asai Y. Kanzawa and T. Takagi (Matsushita Electric Industrial Co., Ltd.)

P1-13 **Influence of roughness with long correlation length on the electron mobility of strained silicon devices** - Isao Kitagawa, Takuya Maruizumi, and Nobuyuki Sugii (Hitachi)

P1-14 **Electrical properties of $Si_{1-y}C_y/Si/SiO_2$ stacks for sub 50nm strained-channel nMOSFETs** - [1,2]F. Ducroquet, [1]T. Ernst, [1,2]O. Weber, [1]J.-M. Hartmann, [1]V. Loup, [3]P. Besson, [1]L. Brévard, [1]J.L. Di Maria, [1]S. Deleonibus ([1]CEA – LETI/DTS – CEA/GRE, [2]LPM, INSA-Lyon, [3]STMicroelectronics)

P1-15 **Analysis of carrier generation lifetime in strained-Si / SiGe heterojunction MOSFETs from capacitance transient** - L.K.Bera, Shajan Mathew, N.Balasubramanian, G. Braithwaite*, M.T. Currie*, F. Singaporewala*, J. Yap*, R. Hammond*, A. Lochtefeld*, M. T. Bulsara*, and E. A. Fitzgerald* (Institute of Microelectronics, *AmberWave Systems Corp.)

P1-16 **Minority Carrier Lifetime and Diffusion Length in $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ Heterolayers** - S. K. Samanta, G. K. Dalapati, S. Chatterjee and C. K. Maiti (IIT)

P1-17 **Electrical Properties of ZrO_2 Films on $Si_{1-x-y}Ge_xC_y$ Epitaxial Layers** - S. Chatterjee, G. K. Dalapati, S. K. Samanta, and C. K. Maiti (IIT)

P1-18 **Low-voltage CMOS operation of SiGe Heterostructure DTMOS** - H. Sorada, A. Inoue, Y. Hara, K. Nozawa, A. Asai, T. Kawashima, K. Katayama, and T. Takagi (Matsushita Electric Industrial Co., Ltd)

P1-19 **Fabrication of 50 nm high performance strained-SiGe pMOSFETs with Selective Epitaxial Growth** - Roger Loo, Matty Caymax, Romain Delhougne, Nadine Collaert, Peter Verheyen** and Kristin De Meyer** (IMEC, **K.U. Leuven)

HBT

P1-20 **Avalanche Considerations in SiGe HBT Scaling** - Greg Freeman, Basanth Jagannathan, Jae-Sung Rieh (IBM Microelectronics)

P1-21 **Emitter Resistance Improvement in High-Performance SiGe HBTs** - Alvin Joseph, Peter Geiss, Xuefeng Liu, Jeffrey Johnson, Kathy Schonenberg*, Ashima Chakravarti*, David Ahlgren*, and James Dunn (IBM)

P1-22 **Self-Aligned Heavily-Boron-Doped SEG SiGe HBT** - Eiji Ohue[1], Yukihiro Kiyota[1], Takashi Hashimoto[1], Tsutomu Udo[2], Akihiro Kodama[3], Hiromi Shimamoto[3], Reiko Hayami[1] and Katsuyoshi Washio[1] ([1]Hitachi Ltd., [2]Hitachi ULSI Systems Co. Ltd., [3]Hitachi Device Engineering Co. Ltd.)

P1-23 **Influence of the Extrinsic Base on the Base Current Kink in SiGe BJTs** - Alexei Sadovnikov, Tracey Krakowski, and Monir El-Diwany (National Semiconductor Corp.)

P1-24 **Design and optimization of a 200 GHz SiGe HBT collector profile by TCAD.** - Andreas D. Stricker, Jeffrey B. Johnson, Greg Freeman, and Jae-Sung Rieh (IBM Microelectronics Division)

P1-25 **The Effect of C on Emitter-Base Design for a Single-Polysilicon SiGe:C HBT with an IDP Emitter** - Erik Haralson, Erdal Suvar, Gunnar Malm, Henry Radamson, Yong-Bin Wang, Mikael Östling (Royal Institute of Technology (KTH))

P1-26 **Characterization of leakage current for SiGeC heterojunction bipolar transistors with a selectively grown collector** - E. Suvar, E. Haralson, H. H. Radamson, Y.-B. Wang, B. G. Malm and M. Östling (Royal Institute of Technology (KTH))

P1-27 **ESD Characterization of SiGe HBT in 0.18-µm SiGe BiCMOS Process** - Shiao-Shien Chen, Tung-Yang Chen, Tien-Hao Tang, Shao-Chang Huang, Tsun-Lai Hsu, Hua-Chou Tseng, Jen-Kon Chen, and Chiu-Hsiang Chou* (United Microelectronics Corporation, *Providence University)

P1-28 **The optimal base design for SiGe heterojunction bipolar transistors with high f_T** - L.S. Lai, Y.H. Liu, C.S. Liang, Y.T. Tseng, Y.M. Shiu, P.S. Chen, S.C. Lu, C.W. Liu and M.-J. Tsai (ITRI)

P1-29 **Low frequency noise behavior of advanced SiGe HBT** - A.Rennane*, L.Bary*, G. Niu**, J.D. Cressler**, J. Joseph***, J.Graffeuil* and R. Plana* (*LAAS-CNRS, **Alabama Microelectronics Science and Technology Center, ***IBM Microelectronics)

P1-30 **Reliability properties of SiGe HBT** - A.Rennane*, L.Bary*, J.L.Roux **, J.Kuchenbecker **, J.Graffeuil* and R. Plana* (*LAAS-CNRS and Université Paul Sabatier, ** CNES)

P1-31 **Achieving a SiGe HBT Epitaxial Emitter with Novel LowThermal Budget Technique** - Paul Brabant, Jianqing Wen, Joe Italiano, Trevan Landin, Nyles Cody and Lee Haen (ASM America Inc.)

P1-32 **Evaluation of Compact Noise Modeling for Si/SiGe HBTs Based on Hierarchical Hydrodynamic Noise Simulation** - M. Bartels , B. Neinhüs , C. Jungemann , B. Meinerzhagen (Universität Bremen)

P1-33 **Comparison of State-of-the-Art Bipolar Compact Models for SiGe-HBTs** - A. Chakravorty, R. Garg, and C. K. Maiti (IIT)

P1-34 **A noise and power analysis of SiGE HBT's for RF applications** - J. Raoult*, J. Verdier*, F. Calmon*, P.J. Viverge**, C. Gontrand* (*Laboratoire de Physique de la Matiè re, **Centre de Génie Electrique de Lyon)

P1-35 **A Direct Extraction Feature for Scattering Parameters of SiGe-HBTs** - S. Wagner[1], V. Palankovski[1], T. Grasser[1], G. Röhrer[2], and S. Selberherr[1] ([1]TU Vienna, [2]AustriamicrosystemsAG)

P1-36 **Rigorous Modeling Approach to Numerical Simulation of SiGe-HBTs** - V. Palankovski[1], G. Röhrer[2], T. Grasser[1], S. Smirnov[1], H. Kosina[1], and S. Selberherr[1] ([1]TU Vienna, [2]AustriamicrosystemsAG)

The Other Devices

P1-37 **Resonant tunneling in Si-SiGe superlattices on relaxed buffer substrates** - S. Tsujino, S. Mentese, L. Diehl, E. Muller, B. Haas, D. Bachli, S. Stutz, H. Sigg, D. Grutzmacher, J. Faist* (Paul Scherrer Institut, *University of Neuchatel)

P1-38 **60nm gate-length Si/SiGe HEMT** - A. Kasamatsu*, K. Kasai*, K. Hikosaka*, T. Matsui* and T. Mimura** (*Communications Research Laboratory, **Fujitsu Laboratories Ltd.)

P1-39 **SiGe virtual substrate HMOS transistor for analogue applications** - K. Michelakis, S. Despotopoulos, V. Gaspari, A. Vilches, K. Fobelets, C. Papavassiliou, C. Toumazou, J. Zhang (Imperial College)

P1-40 **Effect of temperature on the transfer characteristic of a 0.5µm-gate Si:SiGe depletion-mode n-MODFET** - V. Gaspari†, K. Fobelets, J.E. Velazquez-Perez*, R. Ferguson, K. Michelakis, S. Despotopoulos, and C. Papavassilliou (Imperial College London, *Universidad de Salamanca)

P1-41 **Influence of substrate thinning on the threshold voltage of Si:SiGe Heterojunction MOSFETs** - S.M. Li, K. Fobelets , J.E. Velazquez-Perez*, V. Gaspari, R. Ferguson, K. Michelakis, S. Despotopoulos, and C. Papavassilliou (Imperial College London, *Universidad de Salamanca)

P1-42 **Nonvolatile Memory based on Ge/Si Hetero-Nanocrystals** - H.G. Yang, Y. Shi, L. Pu, R. Zhang, B. Shen, P. Han, S.L. Gu, and Y.D. Zheng (Nanjing University)

P1-43 **Si/SiGe heterojunction collector for low loss operation of Trench IGBT** - Tsugutomo Kudoh and Tanemasa Asano (Kyushu Institute of Technology)

P1-44 **Hole-tunneling nanoscale $Si_{0.6}Ge_{0.4}$/Si diode** - Ping Han*, Masao Sakuraba, Junichi Murota, and Youdou Zheng* (* Nanjing University, Tohoku University)

Poster Session (2)
17:25 - 19:00 Thursday, January 16

Strain Control , Epitaxy and Impurity

P2-01 **Development of a new type of SiGe thin strain relaxed buffer based on the incorporation of a carbon-containing layer** - Romain Delhougne, Philippe Meunier-Beillard*, Matty Caymax, Roger Loo, Wilfried Vandervorst (IMEC, *Philips Research Leuven)

P2-02 **Thin strain relaxed SiGe buffer layers on Si and SOI wafers made by He^+ ion implantation and annealing** - S. Mantl[1], B. Holländer[1], N. Hüging[2], M. Luysberg[2], St. Lenk[1], S.M. Hoog[1], H.-J. Herzog[3], T. Hackbarth[3], R. Loo[4], M. Bauer[5] ([1-2]Research Centre Juelich, [3]DaimlerChrysler, [4]IMEC, [5]ASM Germany)

P2-03 **Fabrication SiGe-on-insulator by rapid thermal annealing of Ge thin film on Si-on-insulator substrate** - K.Kutsukake, N.Usami, K.Fujiwara, T.Ujihara, G.Sazaki, B.P.Zhang *and K.Nakajima (Tohoku University, *The Institute of Physical and Chemical Research (RIKEN))

P2-04 **Formation of thin SiGe virtual substrates by ion implantation into Si substrates** - K. Sawano [a], Y. Hirose [b], S. Koh [a], K. Nakagawa [c], T. Hattori [b], and Y. Shiraki [a] ((a) The University of Tokyo, (b) Musashi Institute of Technology, (c) Yamanashi University)

P2-05 **Strain-relaxation mechanisms of SiGe layers formed by two-step growth on Si(001) substrates** - T. Egawa, T. Yamamoto, N. Taoka, O. Nakatsuka, A. Sakai, S. Zaima, and Y. Yasuda (Nagoya University)

P2-06 **Dislocation structures and strain-relaxation in SiGe buffer layers on Si (001) with thin Ge interlayer** - T. Yamamoto, T. Egawa, N. Taoka O. Nakatsuka, A. Sakai, S. Zaima and Y. Yasuda (Nagoya University)

P2-07 **Evaluation of relaxation of strained-Si layers on SiGe-On-Insulator (SGOI) structures after mesa isolation** - Koji Usuda, T.Mizuno, T.Tezuka, N.Sugiyama, Y.Moriyama, S.Nakaharai and S.Takagi (MIRAI Project, ASET)

P2-08 **Influence of SiGe interlayer on the initinal growth of $Si_{1-x-y}Ge_xC_y$ on Si(100)** - S. Ariyoshi, S. Takeuchi, O. Nakatsuka,* A. Sakai, S. Zaima,** and Y. Yasuda (Nagoya University)

P2-09 **Roughening mechanisms of tensily strained $Si_{1-x-y}Ge_xC_y$ films grown by UHV-CVD : a way to maximize substitutional C incorporation** - Cyril Calmes[1], Daniel Bouchier[1], Catherine Clerc[2], Yulin Zheng[3] ([1-2]Université Paris-Sud, [3]Université Paris VI et Paris VII)

P2-10 **Thin, strain relaxed $Si_{1-x}Ge_x$ buffer layers on Si(001) substrates with low defect density and surface roughness** - S.H. Christiansen, P.M. Mooney, J.O. Chu (IBM T.J. Watson Research Center)

Epitaxy

P2-11 **Low temperature H_2 cleaning of Si surface for 0.18-um SiGe-BiCMOS base epitaxy** - T.Tominari, Y.Nonaka, K.Sakai, S.Wada, T.Saito, K.Tokunaga, T.Jimbo, T.Udo*, Y.Kiyota and T.Hashimoto (Hitachi,Ltd., *Hitachi ULSI Systems)

P2-12 **N_2 as carrier gas: an alternative to H_2 for enhanced epitaxy of Si, SiGe and SiGe:C** - P. Meunier-Beillard*, M. Caymax**, K. Van Nieuwenhuysen**, G. Doumen**, B. Brijs**, M. Hopstaken†, L. Geenen** and W. Vandervorst** (*Philips Research Leuven, **IMEC, †Philips Research Laboratories)

P2-13 **Selective Epitaxial Growth of Si and SiGe for MOS transistors** - J.-M. Hartmann, F. Bertin, G. Rolland, F. Laugier, M.N. Séméria, P. Besson and P. Gentile (CEA-DRT – LETI/DTS – CEA/GRE.)

P2-14 **Production-ready Dry Cleaning and Deposition Processes for Low-Temperature Si and SiGe Epitaxy** - Kummer, M. [a], Dommann, A.[a], Buschbaum T. [b], Buschbeck, H. M.[b], Erhart, A.[b], Goeggel, Y.[b], Rosenblad, C. [b], Wiltsche, S.[b], Ramm, J.[b] ((a) Interstate University of Applied Science, (b) Unaxis Semiconductors)

P2-15 **$Si_{1-x}Ge_x$/Si strained epitaxial layer grown by UV/UHV/CVD** - Huiyong Hu, Heming Zhang, Xianying Dai, *Kaicheng Li, Bin Shu, Yi Lv (Xidian University, *National Lab of Analog Ics)

P2-16 **Si/SiGe Selective Epitaxial Growth by a Single-wafer Cold-wall UHVCVD System** - Supika Mashiro, Hiroki Date, Junko Nakatsuru, Satoshi Hitomi, and Junro Sakai (Anelva Corporation)

P2-17 **Carbon incorporation study for SiGeC epitaxy optimization in RTCVD** - F. Deleglise, C. Fellous and D. Dutartre (STMicroelectronics)

P2-18 **Low Temperature, High Growth Rate Epitaxial Silicon and Silicon Germanium Alloy Films** - Michael A. Todd and K. Doran Weeks (ASM America)

P2-19 **Growth of high quality epitaxial $Si_{1-x-y}Ge_xC_y$ layers using chemical vapor deposition** - J. Hallstedt, E. Suvar, P. O. A. Persson*, L.Hultman* and H. H. Radamson (Royal Institute of Technology (KTH), *Linköpings Universitet)

P2-20 **Reduced Pressure Chemical Vapour Deposition of high C content Si / $Si_{1-y}C_y$ heterostructures for n-type MOS transistors** - J.-M. Hartmann, T. Ernst, V. Loup, F. Ducroquet, G. Rolland, P. Holliger, F. Laugier, D. Lafond, M.N. Séméria and S. Deleonibus (CEA-DRT – LETI/DTS – CEA/GRE.)

P2-21 **Reduced Pressure Chemical Vapour Deposition of Si / SiGeC heterostructures using a chlorinated chemistry** - V. Loup, J.-M. Hartmann, G. Rolland, P. Holliger, F. Laugier, D. Lafond and M.N. Séméria (CEA-DRT – LETI/DTS – CEA/GRE.)

P2-22 **Characterization of Ge Gradients in SiGe HBT Test Structures by AES Depth Profile Simulation** - D. Krüger, A. Penkov*, Y. Yamamoto, A. Goryachko**, and B. Tillack (IHP, *National Technical University, **Brandenburg Technical University)

Impurity

P2-23 **High Performance SiGe:C HBTs Using Atomic Layer Base Doping** - Bernd Tillack, Yuji Yamamoto, Dieter Knoll, Bernd Heinemann, Peter Schley, Biswanath Senapati and Dietmar Krüger (IHP)

P2-24 **Enhanced intrinsic Arsenic diffusion in SiGe strained layers.** - A. Pakfar, P. Holliger*, C. Fellous, D. Dutartre. T. Schwartzmann and H. Jaouen. (STMicroelectronics, *CEA-Leti)

P2-25 **On the mechanism of ion- implanted As diffusion in relaxed SiGe** - S. Eguchi, S. J. Rhee[1], D.L. Kwong[1], I. Åberg[2], and J.L. Hoyt [2] (Hitachi Ltd., [1]Univ. of Texas at Austin, [2]MIT)

P2-26 **A new technique to fabricate Ultra-Shallow-Junctions, combining in-situ vapor HCl etching and in-situ doped epitaxial SiGe re-growth** - Roger Loo[1], Matty Caymax[1], Philippe Meunier-Beillard[2], Ivan Peytier[1], Stefan Kubicek[1], Peter Verheyen[1], Richard Lindsay[1], and Olivier Richard[1] ([1]IMEC, [2]Philips Research Leuven)

P2-27 **In-situ B doping of SiGe(C) using BCl_3 by hot-wall LPCVD** - Yasuo Kunii, Yasuhiro Inokuchi, Atsushi Moriya and Harushige Kurokawa ,Junichi Murota* (Hitachi Kokusai Electric Inc., *Tohoku University)

P2-28 **Low-Temperature Dopant Activation Technology Using Elevated Ge-S/D Structure** - Hideki Takeuchi, Pushkar Ranade and Tsu-Jae King (University of California at Berkeley)

P2-29 **Relationship between Total Impurity(B or P) and Carrier Concentrations in SiGe Epitaxial Film Produced by the Thermal Treatment** - Jintae Noh, Shinobu Takehiro, Masao Sakuraba and Junichi Murota. (Tohoku University)

P2-30 **Characterization of As^+-ion-implanted layers in strained-Si/SiGe/Si hetero-structures** - T. Ishida*,T. Inada**, N. Sugii*** and S.Irieda* (*Hosei University, **Hosei University Reserch Institute, ***Hitachi Ltd.)

P2-31 **Segregation of Boron to Polycrystalline and Single-crystal $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ Layers** - E. J. Stewart and J. C. Sturm (Princeton University)

P2-32 **High Resolution Depth Profiling of Dopants in SiGe on Si (001)** - N.L Rowell*, D.C. Houghton**, M. Ward***, and D. Webb*** (*National Research Council of Canada, **AIXTRON Inc., ***ATMI Corp.)

Process Tech.

P2-33 **Reactive Ion Etching of $Si_{1-x}Ge_x$ Alloy with Hydrogen Bromide** - C. S. Wang, D. Y. Shu, C. M. Liu, and M.-J. Tsai (ITRI)

P2-34 **Etching Characteristics of Impurity-Doped $Si_{1-x}Ge_x$ Epitaxial Films Using Electron-Cyclotron-Resonance Chlorine Plasma** - Hang-Sup Cho, Shinobu Takehiro, Masao Sakuraba and Junichi Murota. (Tohoku University)

P2-35 **Ge dependent morphological change in poly-SiGe formed by Ni-mediated crystallization** - H. Kanno, I. Tsunoda, A. Kenjo, T. Sadoh, and M. Miyao (Kyushu University)

P2-36 **Enhanced growth of amorphous interlayer in Ti thin films on strained Si/SiGe relaxed substrates** - H. C. Chen, S. W. Lee, S. L. Cheng, L. J. Chen, P. S. Chen* and C. W. Liu* (National Tsing Hua University, *ITRI)

P2-37 **Enhanced crystal nucleation in a-SiGe/SiO_2 by ion-irradiation assisted annealing** - I. Tsunoda, A. Kenjo, T. Sadoh, and M. Miyao (Kyushu University)

Quantum Dot

P2-38 **Selective epitaxial growth of Ge quantum dots on patterned Si(001) surfaces** - Lam. H. Nguyen*, V. Le Thanh, V. Yam, D. Débarre, M. Halbwax, D. Bouchier (Université Paris-Sud)

P2-39 **Shape and composition change of Ge dots due to Si capping** - O. Kirfel[1], E. Mü ller[1], D. Grützmacher[1], K.Kern[2], A.Hesse[3], J. Stangl[3], V. Holý[3], G. Bauer[3] ([1]Paul Scherrer Institut, [2]École Polytechnique Fédérale de Lausanne, [3]University of Linz)

P2-40 **Self-Organized Ge/Si Islands Grown by a Homemade UHV/CVD System** - Jinzhong YU, Changjun HUANG, Buwen CHENG, Yuhua ZUO, Liping LUO, Zhenglin LEI and Qiming WANG (Institute of Semiconductors, Chinese Academy of Sciences)

P2-41 **Kinetics of Ge quantum islands capping by silicon** - V. Yam, V. Le Thanh, D. Débarre and D. Bouchier (Université Paris-Sud)

P2-42 **Optical Properties of Stacked Ge/Si Quantum Dots with Different Spacer Thickness Grown by Chemical Vapor Deposition** - W. Y. Chen, W.-H. Chang, A. T. Chou, T. M. Hsu, P. S. Chen*, Zingway Pei* and L. S. Lai* (National Central University, *ITRI)

P2-43 **Novel composite Ge/Si/Ge quantum dots with high PL efficiency and improved uniformity** - P. S. Chen, S. W. Lee, Y. H. Peng, Z. Pei, M. –J. Tsai ,C. W. Liu (ITRI)

P2-44 **Improved quality of Ge quantum dots in Ge/Si stacked layers by pre-intermixing treatments** - S. W. Lee[1.2], P. S. Chen[2], Y. H. Peng[2], C. W. Liu[2] and L. J. Chen[1] ([1]National Tsing Hua University, [2]ITRI)

P2-45 **Influence of Thermal Annealing on Compositional Mixing and Crystallinity of Highly-Selective Grown Si Dots with Ge Core** - Yudi Darma, Hideki Murakami and Seiichi Miyazaki (Hiroshima University)

P2-46 **Synthesis of Ge nanowires using Au nanoparticles catalyst on alumina template** - Ye Zhizhen, Wu Guibin Huang Jingyun, CuiJiFeng, Zhao Binghui (Zhejiang University)

P2-47 **Coupling effect dependent on the thickness of the spacer layer between double layer of Ge quantum dots embedded in Si** - Yin Rao, Qi Gao, Zuimin Jiang and Fang Lu (Fudan University)

P2-48 **Reduced Pressure Chemical Vapour Deposition of Ge quantum dots** - J.-M. Hartmann, F. Bertin, G. Rolland and M.N. Séméria (CEA/GRE - LETI/DTS/STME/L2TI)

Optical Devices

P2-49 **Room Temperature 1.3 and 1.5 μm Electroluminescence from Si/Ge Quantum Dots (QDs)/Si Multi-layers** - Z.Pei, P.S.Chen, L.S.Lai, S.C. Lu , M.-J. Tsai, W. H. Chang*, W.Y. Chen*, A.T. Chou*, and T.M. Hsu* (ITRI, *National Central University)

P2-50 **High Speed Lateral PIN Germanium-on-Silicon Photodetectors** - G. Dehlinger, J. D. Schaub, J. O. Chu, S. J. Koester, Q. C. Ouyang and A. Grill (IBM)

P2-51 **SiGe PIN photodetector for infrared optical fiber links operating at 1.25 Gbit/s** - M. Jutzi[1], M. Berroth[1], G. Wöhl[2], C. Parry[2], E. Kasper[2] (Univ. Stuttgart)

P2-52 **2×2 Electrooptical Switch with SOI Waveguide** - Jinzhong YU, Qingfeng YAN, Jinsong XIA, Zhongchao FAN, Zhangtao WANG, Shaowu CHEN (Institute of Semiconductors)

P2-53 **Long-wavelength SiGe/Si MQW Resonant-Cavity-Enhanced photodetectors (RCE-PD) for application in Optical Fiber Communication Network** - Qiming Wang, Cheng Li, Buwen Cheng, Qinqing Yang, Zhenglin Lei and Jinzhong Yu (Institute of Semiconductors)

P2-54 **Fabrication of Epitaxial SiGe Optical Waveguide Structures** - Yihwan Kim, Dean Berlin, and Arkadii Samoilov (Applied Materials Inc.)

P2-55 **Schottky Quantum Dots Infrared Photodetector with Far Infrared Response** - Y. H. Peng[1], Jen-Hsiang Lu[1], C. H. Kuan[1], C. W. Liu[1], Pang-Shiu Chen[2], Z. Pei[2], M.–J. Tsai[2], S. W. Lee[3], L. J. Chen[3], M. H. Ya[1], Y. F. Chen[1] ([1]National Taiwan University, [2]ITRI, [3]National Tsing Hua University)

Poster Session (3)
17:20 - 18:40 Friday, January 17

New Technique

P3-01 **Si Atomic Layer Epitaxy from Thermally Cracked Si_2H_6 (TCH-ALE) and the mechanisms of the adsorption process** - Yoshiyuki Suda and Kazushi Miki* (Tokyo University of Agriculture and Technology, *National Institute of Advanced Industrial Science and Technology)

P3-02 **GeH_4 adsorption on Si(001) at room temperature: transfer of H atoms to Si sites and atomic exchange between Si and Ge** - Takeshi Murata, Maki Suemitsu (Tohoku University)

P3-03 **Si self-diffusion in heavily B-doped epitaxial silicon** - K. Toyonaga[1], S. Rahamah Bt Aid[1], Y. Nakabayashi[1], S. Matsumoto[1], M. Sakuraba[2], Y. Shimada[2], A. Hashiba[2], and J. Murota[2] ([1]Keio University, [2]Tohoku University)

P3-04 **Adsorption kinetics of dimethylsilane on Si(001)** - K.Senthil[1], H.Nakazawa[2] and M.Suemitsu[1] ([1]Tohoku University, [2]Hirosaki University)

P3-05 **Kinetics of Epitaxial Growth of Si and SiGe films on (110) Si Substrates** - N. Sugiyama, Y. Moriyama, S. Nakaharai, T. Tezuka, T. Mizuno and S. Takagi (MIRAI project, ASET)

P3-06 **Local atomic structure in Czochralski-grown $Ge_{1-x}Si_x$ bulk alloys** - I. Yonenaga, M. Sakurai, M. H. F. Sluiter and Y. Kawazoe (Tohoku University)

P3-07 **Epitaxial Growth of N Delta Doped Si Films on Si(100) by Alternately Supplied NH_3 and SiH_4** - Youngcheon Jeong, Masao Sakuraba and Junichi Murota (Tohoku University)

P3-08 **Gas Control Technologies for SiGe deposition processes** - Nobuyasu Tomita, Hiroyuki Ono, Takuya Ikeda, Yoshiaki Sugimori and Satoshi Hasaka (Nippon Sanso Co.)

P3-09 **Formation of Heavily P Doped Si Epitaxial Film on Si(100) by Multiple Atomic-Layer Doping Technique** - Yosuke Shimamune, Masao Sakuraba and Junichi Murota* (Tohoku University)

P3-10 **Carbon Effect on Thermal Stability of Si Atomic Layer on Ge(100)** - Masaki Fujiu, Kazuya Takahashi, Masao Sakuraba and Junichi Murota* (Tohoku University)

P3-11 **Ar Plasma Irradiation Effects in Atomically Controlled Si Epitaxial Growth** - Daisuke Muto, Masao Sakuraba*, Takuya Seino and Junichi Murota (Tohoku University)

Circuit Technology

P3-12 **Static Frequency Divider Circuit using Strained SiGe p-MODFETs** - D. V. Singh, S. J. Koester, J. O. Chu, K. A. Jenkins, P. M. Mooney, Q. C. Ouyang, N. Ruiz, J. A. Ott, D. Ralston*, M. Wetzel*, P. M. Asbeck*, V. V. Patel, and A. Grill (IBM Research Division, *University of California)

P3-13 **SiGe based Low Noise Amplifier for WLAN applications** - J.Sadowy[1, 2], V.Le-Goascoz[2], I.Telliez[2], J.Graffeuil[1], E.Tournier[1], L. Escotte[1] and R. Plana[1]. ([1]LAAS-CNRS, [2]STMicroelectronics)

P3-14 **The Comparison of Isolation Technologies and Device Models on SiGe Bipolar Low Noise Amplifier** - W.-C. Hua[a], T.-Y. Yang[b], C. W. Liu[a,b] ([a]National Taiwan University, [b]STC/ITRI)

P3-15 **Design of a 4.4-5 GHz LNA in 0.25-µm SiGe BiCMOS Technology** - Paolo Crippa, Simone Orcioni, Francesco Ricciardi, and Claudio Turchetti (University of Ancona)

P3-16 **Design of a DC-5 GHz MOS-based SPDT T/R Switch in 0.25-µm SiGe BiCMOS Technology** - Paolo Crippa, Simone Orcioni, Francesco Ricciardi, and Claudio Turchetti (University of Ancona)

P3-17 **A 2.9GHz-Band SiGe-MMIC On-Chip VCO** - Yasuhiro Nabeno, Masayoshi Ono, Takayuki Sugano, Masahiko Nakanishi, Noriharu Suematsu (Mitsubishi Electric Corp.)