



6th International Symposium on Control of Semiconductor Interfaces

May 25(Wed)-27(Fri), 2011

Research Institute of Electrical Communication

Tohoku University, Sendai, Japan

Web site: [http:// www.murota.riec.tohoku.ac.jp/ISCSI6/](http://www.murota.riec.tohoku.ac.jp/ISCSI6/)

The Sixth International Symposium on Control of Semiconductor Interfaces (ISCSI-VI) will be held at Tohoku University in Sendai, Japan, on May 25-27, 2011. ISCSI was established by the 154 Committee on Semiconductor Interfaces and Their Application, the University-Industry Cooperative Research Committee, The Japan Society for the Promotion of Science (JSPS), following a series of highly successful meetings held at Karuizawa, Japan, in 1993, 1996, 1999, 2002, and at Hachiohji, Japan, in 2007. The aim of this symposium is primarily to bring together leading-edge researchers and other interested parties in the field of science and engineering of semiconductor interfaces and related matters.

ISCSI-VI will be collocated with the 7th International Conference on Silicon Epitaxy and Heterostructures (ICSI-7), May 22(Sun)-26(Thu), 2011. Some focus sessions will be jointed with ICSI-7.

Topic Areas

Thin Film Growth and Characterization

Si, Strained Si, Ge, SiGe(C), SiC, Diamond, Silicide, Compound semiconductors, III-nitrides, Oxide semiconductors, High-k insulator, Low-k insulator
CVD, MBE, Selective epitaxy, Atomic layer control, Novel growth technique
Band engineering, Defect engineering, Simulation and modeling

Surface and Interface Control

Surface passivation and modification, Surface and interface chemistry
Schottky and ohmic contacts
Atomic scale characterization of surfaces and interfaces
Surface/interface issues in advanced devices

Formation and Characterization of Nanostructures

Nanodots, Nanowires, Superlattice
Self-assembling, Self-organization
Nanoscale characterization, In-situ characterization

Process and Device Technology

Impurity diffusion, Dry etching, Microfabrication, Isolation
SiGe gate, Source/drain and channel engineering, Base/emitter engineering
SOL, SGOI, III-V on Si, Wafer bonding, Virtual substrates and their Manufacturing
CMOS, HBT, BiCMOS, FeRAM, MODFET, SET, RTD, LED, LD, OEIC

Submission of Papers

Paper acceptance is based on abstract submission. The work must be original and unpublished. Prospective authors should submit abstract(s) (only in PDF file), two pages in length including all figures and tables, by **February 15, 2011 (extended)**, to a submission World Wide Web site (the site information will be announced at the above symposium web site). The two-page abstract must be written in English and typed in an area of 8.5 x 11 inches or A4 size. The first page must be headed by the title of the paper, author(s), affiliation(s), address, telephone number, fax number, e-mail address of the corresponding author. The text of the abstract must clearly and concisely state the specific results of the work and its originality. Please refer to the sample abstract (PDF file at the above symposium web site) for detailed format information. If you use, please download the abstract template (Microsoft Word at the above symposium web site) and prepare your abstract following the instructions. **Proceedings will be published in the special issue of Thin Solid Films (manuscript submission deadline will be around middle of May, 2011).** Detailed information will be announced on the above symposium web site.

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