Logical Operations exploiting Stochastic Resonance for Coarse-Grained Devices

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Abstract: Noise and fluctuations are usually considered obstacles in the operation of both analog and digital computing systems, and most strategies to deal with them focus on suppression. Neural systems, on the other hand, tend to employ strategies in which the properties of noise are exploited to improve the efficiency of operations. This concept may be especially useful in the design computing systems with noise-sensitive devices (e.g., extremely low-power devices like single-electron, molecular, subthreshold analog CMOS devices, etc.). This talk gives an overview of noise-driven information processing and their possible applications in electronics. Stochastic resonance (SR) is a phenomenon where a static or dynamic threshold system responds stochastically to a subthreshold or suprathreshold input with the help of noise. In biological systems SR is utilized to detect weak signals under a noisy environment. SR on some emerging research devices (single-electron devices, GaAs nanowire FETs, etc.) has been demonstrated [1,2]. SR can be observed in many bi-stable systems, and will be utilized to facilitate the state transitions in emerging logic (bi-stable) memory devices. Noise-driven fast signal transmission is observed in neural networks for the vestibulo ocular reflex, where signals are transmitted with an increased rate over a neuronal path when non-identical neurons and dynamic noise are introduced. Implementation in terms of a single electron circuit has demonstrated that when several non-identical pulse-density modulators were used as noisy neurons, performances on input-output fidelity of the population increased significantly as compared to that of a single neuron circuit [3]. Phase synchronization among isolated neurons can be utilized for skew-free clock distribution where independent oscillators are implemented on a chip as distributed clock sources, while the oscillators are synchronized by a common temporal noise. Noise in synaptic depression can be used to facilitate the operation of a neuromorphic burst-signal detector, where the output range of the detector is significantly increased by noise. Noise-shaping in inhibitory neural networks has been demonstrated in subthreshold CMOS, where static and dynamic noises can positively be taken if one could not remove a certain level of noise or device mismatches. The circuits exploit properties of device mismatches and external (temporal) noise to perform noise-shaping 1-bit AD conversion (pulse-density modulation). These examples demonstrated that the noise-driven computing strategies would be important in the designs of emerging computer architectures consisting of nanometer-scale, noise-sensitive, and coarse-grained devices and materials.

Keywords: nanoelectronics, information processing, neuromorphic computing, emerging research architecture

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