Atomic Scale Processing of Ultra-thin Barriers for Advanced Interconnects

Daniel Greenslit, Tonmoy Chakraborty, and Eric Eisenbraun
The College of Nanoscale Science and Engineering
The University at Albany-SUNY
257 Fuller Rd., Albany, New York 12203
Phone: 518.437.8686 Fax: 518.437.8603
eeisenbraun@albany.edu

In traditional semiconductor technology a sputtered copper seed layer is used to improve the adhesion, microstructure, and electromigration characteristics of electrochemically deposited (ECD) copper. The seed layer is deposited on top of a Ta/TaN stack. The TaN serves as a diffusion barrier and the Ta layer acts as an adhesion and nucleation layer for the copper seed [1]. This PVD Cu/Ta/TaN stack is relatively thick, and the scaling of interconnects is making the development and commercialization of a barrier layer that can be direct plated without the need for a seed layer increasingly attractive. Materials under consideration for direct plating include Ru, Pt, and Ir, but none of these possess robust diffusion barrier characteristics[2]. Similarly, materials traditionally used as diffusion barriers, such as TaN or TaSiN are not suitable for direct plating[3].

This presentation will describe details of research that has revealed that mixed phase materials composed of selected components such as Ru/TaN and Ru/Co, grown by plasma enhanced atomic layer deposition (PEALD), act both as a directly platable surface and as a Cu diffusion barrier[4]. Figure 1 is a cross-section scanning electron micrograph (SEM) emonstrating complete fill of a high aspect ratio trench structure with Cu plated directly on the barrier with no seed layer. This single layer, which has been observed to be extendible to thicknesses as small as ~2-3nm, offer a potential solution for sub-28nm interconnect technologies, where more traditional copper barrier/seed approaches are not able to maintain required performance characteristics.

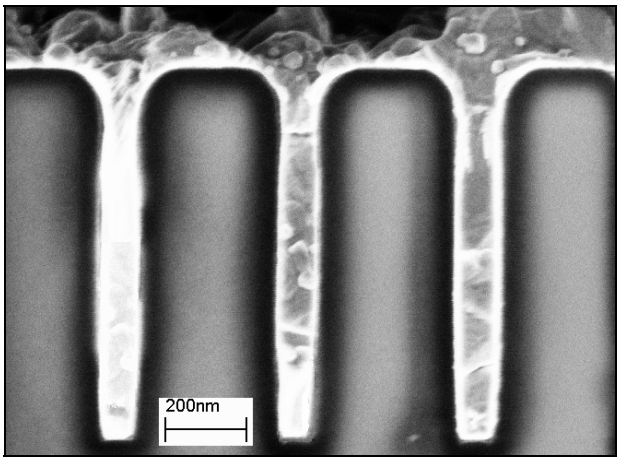

Fig. 1 Direct plating of copper on 5nm thick PEALD-grown RuTaN liner with no Cu seed layer.

References

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