

# Fabrication of single-electron transistors with a self-alignment process using anodization of aluminum microelectrodes"

Michio Niwano and Yasuo Kimura

Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication,  
Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai 980-8577, Japan  
niwano@riec.tohoku.ac.jp

Fabrication of nanostructures has so far been extensively studied in order to develop electronic or photonic devices which work with new operating principles such as quantum effects. There are generally two complementary approaches to the fabrication of nanostructures on solid substrates. One is a top-down process which is typified by the conventional lithographic technique widely used in Si LSI technology, and the other is a bottom-up process such as a self-organization process. For a lithographic technique, it is not easy to fabricate nanostructures, while we can put elemental devices at desired positions on solid substrates. For a self-organization process, on the other hand, it is not easy to put nanostructures at desired positions on substrates, while we can easily form nano-scaled structures. Therefore, it is required for the fabrication of practical nanodevices to develop a hybrid process in which these complementary techniques are combined.

It is well-known that anodization of aluminum plates or films produces porous anodic alumina having the self-ordered nanohole arrays [1]. Previously, a Coulomb blockade phenomenon has been observed at room temperature for nanodots or nanowires of cadmium sulfide or zinc selenide that were formed in the nanoholes of porous anodic alumina [2]. Although the positions of those nanodots or nanowires were not controllable, this observation showed that porous anodic alumina may be used as a template for nanostructure formation. In this study, we investigate a method of forming aluminum (Al) nanodots with their positions being controlled by using a hybrid process in which an anodization process for porous alumina formation is combined with a photolithographic technique. We used the hybrid process to fabricate the single-electron-transistor (SET) structure, and examined the electron transport characteristics of the SET structure thus fabricated [3].

Aluminum nanodots are self-organized on a substrate by anodizing an aluminum thin film deposited on the substrate [4, 5]. In our method, we can control the position of those aluminum nanodots by anodizing a restricted portion of an aluminum microelectrode by means of a photolithography technique, as is illustrated in Fig. 1. The inset of Fig. 1 shows a cross-sectional view of a porous anodic alumina layer and aluminum nanodots formed by partial anodization of the aluminum microelectrode.

A p-type silicon (100) wafer was used as a substrate. A 500-nm thick aluminum film was evaporated onto a 100-nm thick silicon dioxide layer formed on the silicon substrate surface. The aluminum film was etched using a photolithographic technique to form an aluminum microelectrode of 3  $\mu\text{m}$  in width. The microelectrode was then covered with a 200-nm thick silicon oxide ( $\text{SiO}_x$ ) layer with the center region of the microelectrode being uncovered. Finally, the uncovered area of the electrode was anodized in a sulfuric acid solution of 1.7 % at an anodic potential of 25 V.

Figure 2 shows the I-V characteristics of the anodized microelectrode, which were measured at room temperature. A clear staircase current was observed at source-drain voltages of 2 and 6 V, which indicates that a Coulomb blockade phenomenon took place in our SET structure. The Coulomb energy was about 2 eV, which is

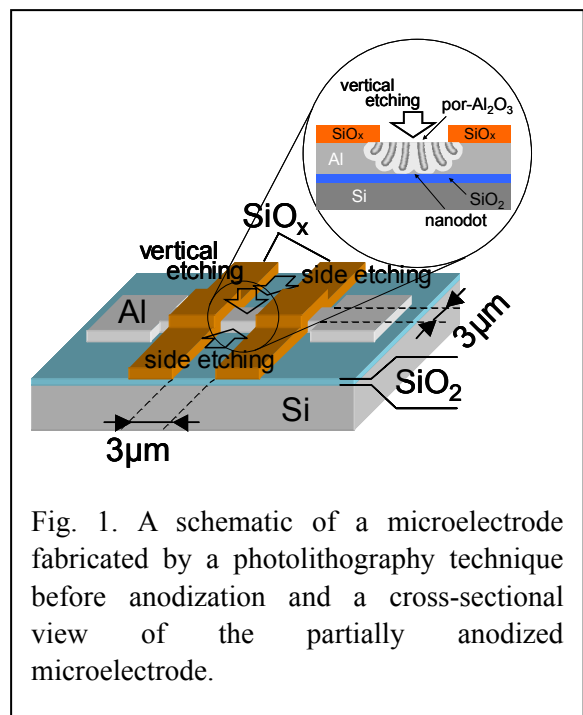


Fig. 1. A schematic of a microelectrode fabricated by a photolithography technique before anodization and a cross-sectional view of the partially anodized microelectrode.

the largest among the values found in our literature survey. A total capacitance of this SET structure is estimated to be about 0.04 aF, which corresponds to a capacitance of parallel plate electrodes with an area of  $2.3 \times 2.3 \text{ nm}^2$  and a gap of 10 nm. The small capacitance is attributed to the structure of electrodes and nanodots formed by anodization.

Figure 3(a) shows a cross-sectional field emission scanning microscope (FE-SEM) image of a porous alumina layer formed by partially anodizing an aluminum film. We can see that in the porous anodic alumina layer, bended pores grow around the edges of the  $\text{SiO}_x$  mask window, while straight pores grow in the direction perpendicular the substrate surface around the center of the  $\text{SiO}_x$  mask window. Since the growth rate of straight pores is larger than that of bended pores, porous alumina around the center grow more quickly than that around the edge regions. Thus, the metallic Al electrode would be very thin at the center region where Al nanodots form as is depicted in the inset of Fig. 1. The inset of Fig. 3(a) shows a magnified image of the interfacial region between the porous alumina layer and the Si substrate. We can see Al nanodots are present in the interface. In order to observe Coulomb staircases, it is additionally required to fabricate narrow and thin source and drain electrodes because those electrodes decrease a total capacitance of the SET structure. Figure 3(b) shows a FE-SEM image of the microelectrode after anodization. We can see a nanowire of about 100 nm in width was formed. Note that the initial width of the electrode was 3  $\mu\text{m}$ . We think side etching of the microelectrode took place along with vertical etching because the sides of the microelectrode was not covered with the  $\text{SiO}_x$  film. Accordingly, we conclude that the observed thinning and narrowing of the microelectrode reduced the capacitance of the SET structure, leading to a very large Coulomb energy.

In summary, the present results indicate that a hybrid technique in which self-organization and lithography techniques are combined, provides a powerful tool to fabricate nano-scaled electronic devices that cannot be fabricated solely through the conventional lithographic technique.

## References

- [1] H. Masuda, K. Nishio, and N. Baba, *J. Mater. Sci. Lett.* **13** (1994) 338.
- [2] N. Kouklin, L. Menon, and S. Bandyopadhyay, *Appl. Phys. Lett.* **80** (2002) 1649.
- [3] Y. Kimura, K. Itoh, R. Yamaguchi, K. Ishibashi, Kingo Itaya and M. Niwano, *Appl. Phys. Lett.* **90** (2007) 093119.
- [4] S. Shingubara, Y. Murakami, H. Sakaue and T. Takahagi, *Jpn. J. Appl. Phys.* **41** (2002) L340.
- [5] Y. Kimura, H. Shiraki, K. Ishibashi, H. Ishii, K. Itaya, and M. Niwano, *J. Electrochem. Soc.* **153** (2006) C296.

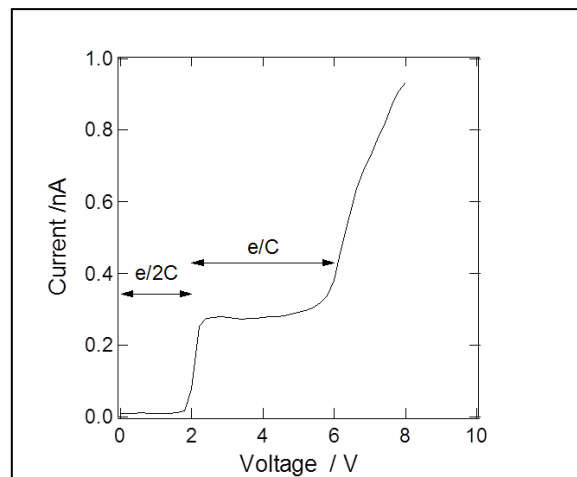


Fig. 2. I-V characteristics for a SET structure fabricated by both anodization process and a lithography technique.

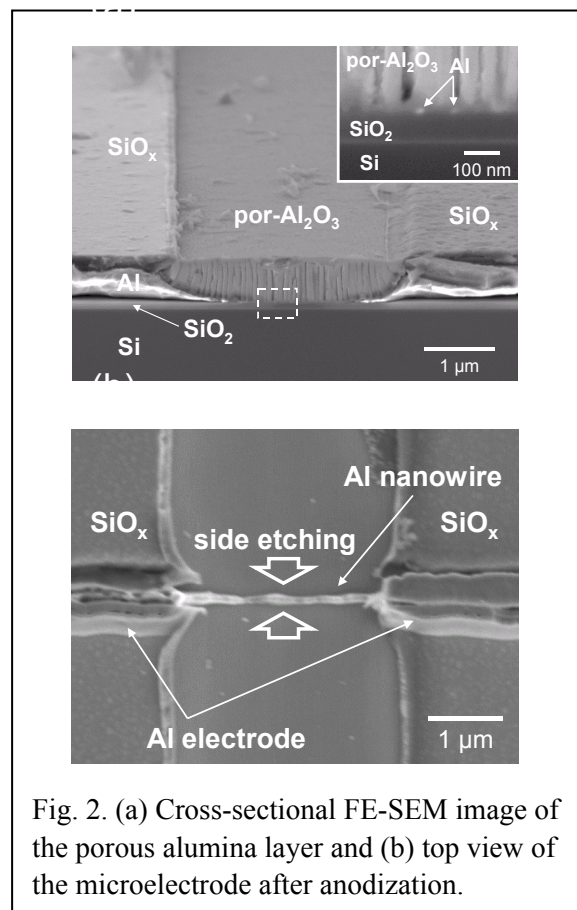


Fig. 2. (a) Cross-sectional FE-SEM image of the porous alumina layer and (b) top view of the microelectrode after anodization.